



SDH synchronization



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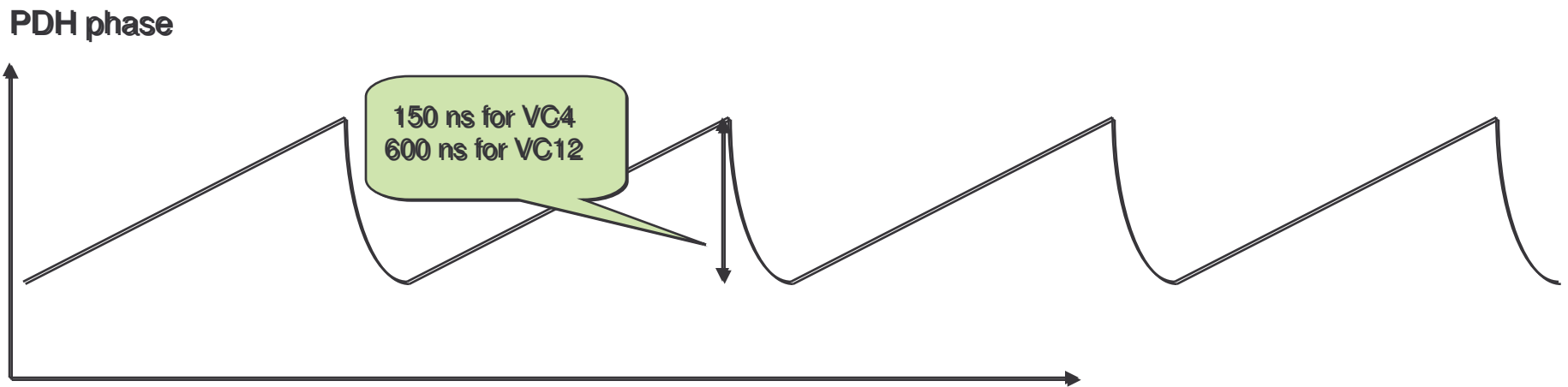
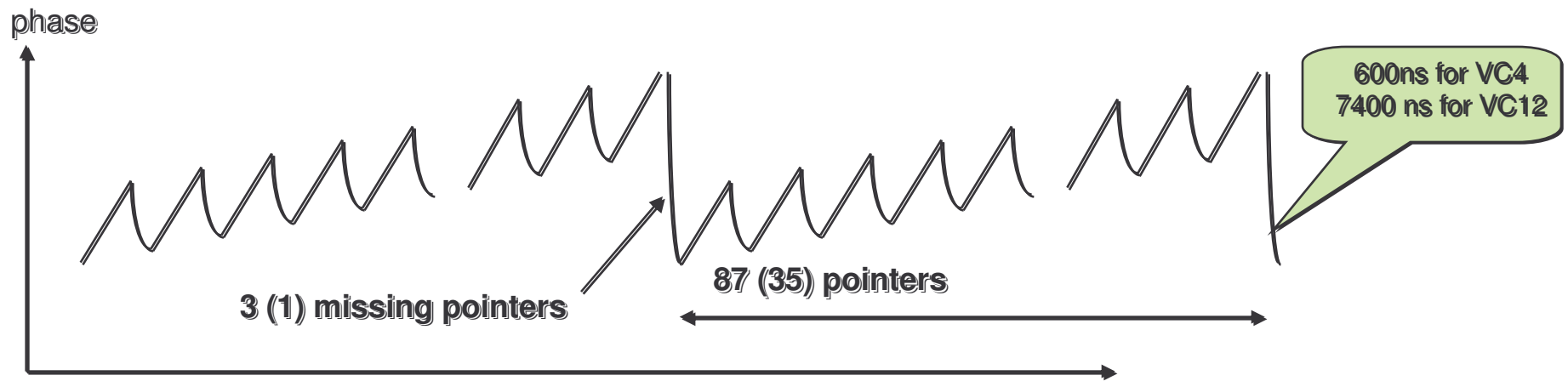
SDH synchronization

- > **Basics of SDH**
- > Why do SDH network needs synchronization?
- > How to synchronize SDH networks
 - SDH master-slave synchronization architecture
 - SETS timing modes and SEC-SSU interworking, intra-node architecture
 - Intra-node architecture
 - SSM and ring architecture
- > Inter-node architecture options
 - Hierarchical master-slave, distributed and hybrid solutions
- > Synchronization of E1 layer and retiming

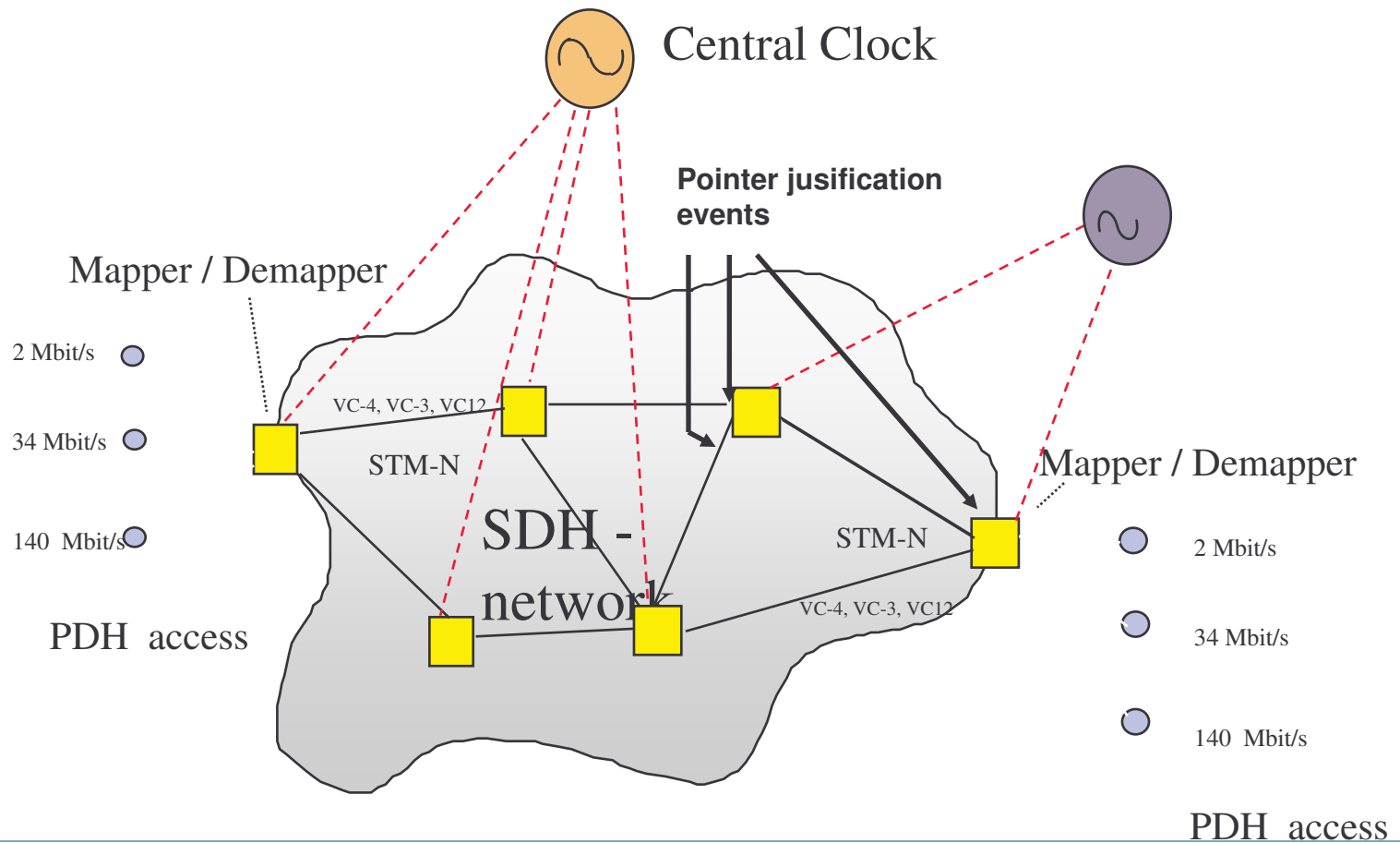
SDH basics

- > The SDH Frame transports a PDH payload within VCs aligned in TUs and AUs with pointers
 - VC12 carrying 2 Mbit/s tributary are aligned in TU12 via a 1 byte pointer
 - TU12 are multiplexed into TUG 2 & 3 then mapped into VC4
 - VC4 are aligned in AU4 via a 3 byte pointer
- > These VC12 pointers carry traffic data or not depending on the frequency alignment of VC12 and TUs, generating Pointer Justification Events (PJE), then phase gaps of 3.7 microseconds on the 2 Mbit/s signal recovered after being extracted (desynchronized) from the VC12
- > The SDH frame carries a SSM, Synchronous Status Message that is used for synchronizing the SDH network

sequences of pointers



SDH Network Synchronisation Mapping & PJE due to desynchronisation



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Why synchronizing SDH networks (1)?

- >The G.707 frame has internal mechanisms, called pointer processors, that allow SDH to work in a non synchronized environment.
 - Pointers allow desync between 2 equipments without significant effect on the PDH payload (although some problems appeared at the beginning of SDH (35/1 effect) deployment in the fields, which have been solved 10 years ago)
 - Within an SDH network, there is no problem in the SDH frame in case of any case of desynchronization, even if all NEs are desynchronized.

- >**But**, Accumulation of pointers due to multiple desynchronization
 - may generate excessive jitter and wander on PDH payload
 - May generate LOF on PDH payload due to buffer overflow or underflow

Why synchronizing SDH networks ? (2)

- > Transport of synchronization within SDH
 - Before SDH, synchronization was transported via 2 Mbit/s E1 signals.
 - Introduction of SDH in the networks might corrupt the timing quality of 2 Mbit/s signals, making them unable to transport synchronization if transported via a SDH VC12 with PJE.
 - The transport of synchronization through SDH networks is done using the STM-N signals, which timing is regenerated in each SDH NE terminating a multiplex section.
 - synchronization of SDH NEs is required to transport timing via STM-N signals in an SDH network
 - It will be shown later how to insert and extract synchronization from an SDH network

SDH synchronization

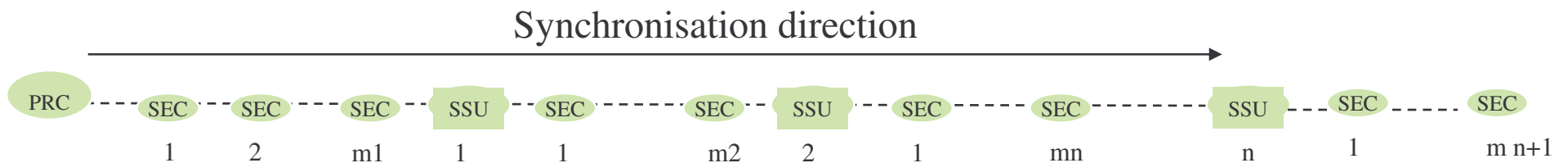
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How to synchronize SDH networks

- It must be possible to provide synchronization to SDH and to transport this synchronization between the SDH NEs
- SDH NEs must be able to receive timing from reference sources
 - via dedicated external ports
- Transport of timing by the STM-N signals
 - Noise is accumulated along the chain of clocks. This is a major issue for transporting timing via STM-N signals
 - Solutions
 - masterslave sync architecture
 - Hierarchical clocks
 - clock for the SDH NEs
 - SSM in G.707

SDH Network Synchronisation

Synchronisation reference chain



Maximum numbers according to G.803:

- maximum number of SEC's between 2 SSUs: $m_1, m_2, \dots, m_{n+1} \leq 20$
- maximum number of SSU's in a chain: $n \leq 10$
- maximum number of SEC's in a chain: 60

Clock types

> 3 types of clock

- G.811 Primary Reference Clock (PRC)
 - Accuracy: 10^{-11}
- G.812 Synchronization Supply Unit (SSU)
 - Holdover: ageing per day $2 \cdot 10^{-10}$
 - Bandwidth 3 mHz
- G.813 SDH Equipment Clock (SEC)
 - Accuracy $4.6 \cdot 10^{-6}$
 - Holdover: ageing per day, 10^{-8}
 - Bandwidth 1-10 Hz

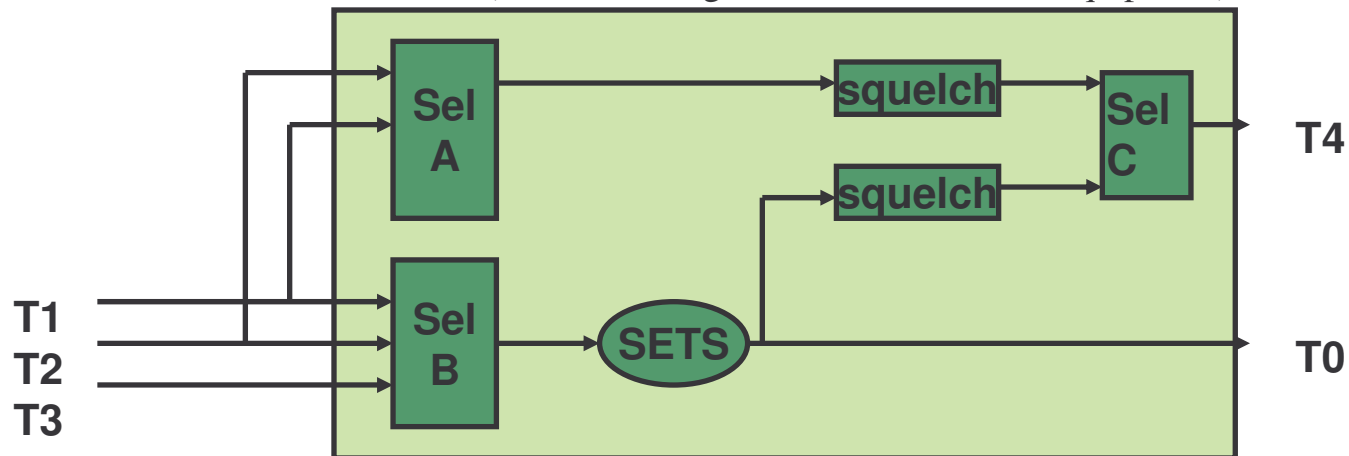
> The bandwidths have been defined in order to maintain Jitter and Wander within specified limits

SEC (SDH Equipment Clock)

> Block diagram of an SEC

- 2 output types, T0 and T4

T3 : 2MHz input sync. Signals (may be derived from 2 Mbit/s without traffic)
T4 : 2MHz output sync. Signals (may be derived from 2 Mbit/s without traffic)
T1 : 2 Mhz derived from STM-N
T2 : 2 MHz derived from 2 Mbit/s
T0 : 2 MHz station clock (delivers timing to all functions of the equipment)



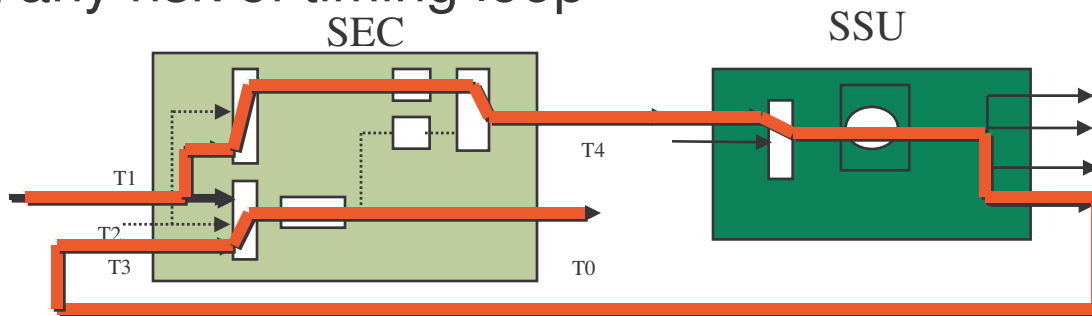
SETS: SDH Equipment Timing Source

SETS timing modes

- Line timing
 - The SEC gets its timing from the East or West line signal
- Tributary timing
 - The SEC gets its timing from a tributary port, STM-N or PDH
- External timing
 - The network element uses an external reference signal dedicated for synchronization (without traffic). Signal types: 2 048 kHz or 2 048 kbit/s
- Internal timing
 - The clock of the NE is not locked to a reference signal, in free-run and holdover modes

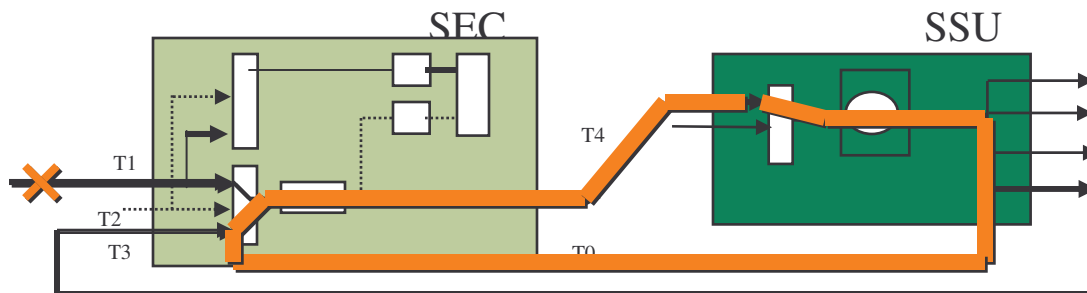
SEC-SSU interworking

- > Using the T1-T4 link allows to synchronize the SEC from the SSU without any risk of timing loop



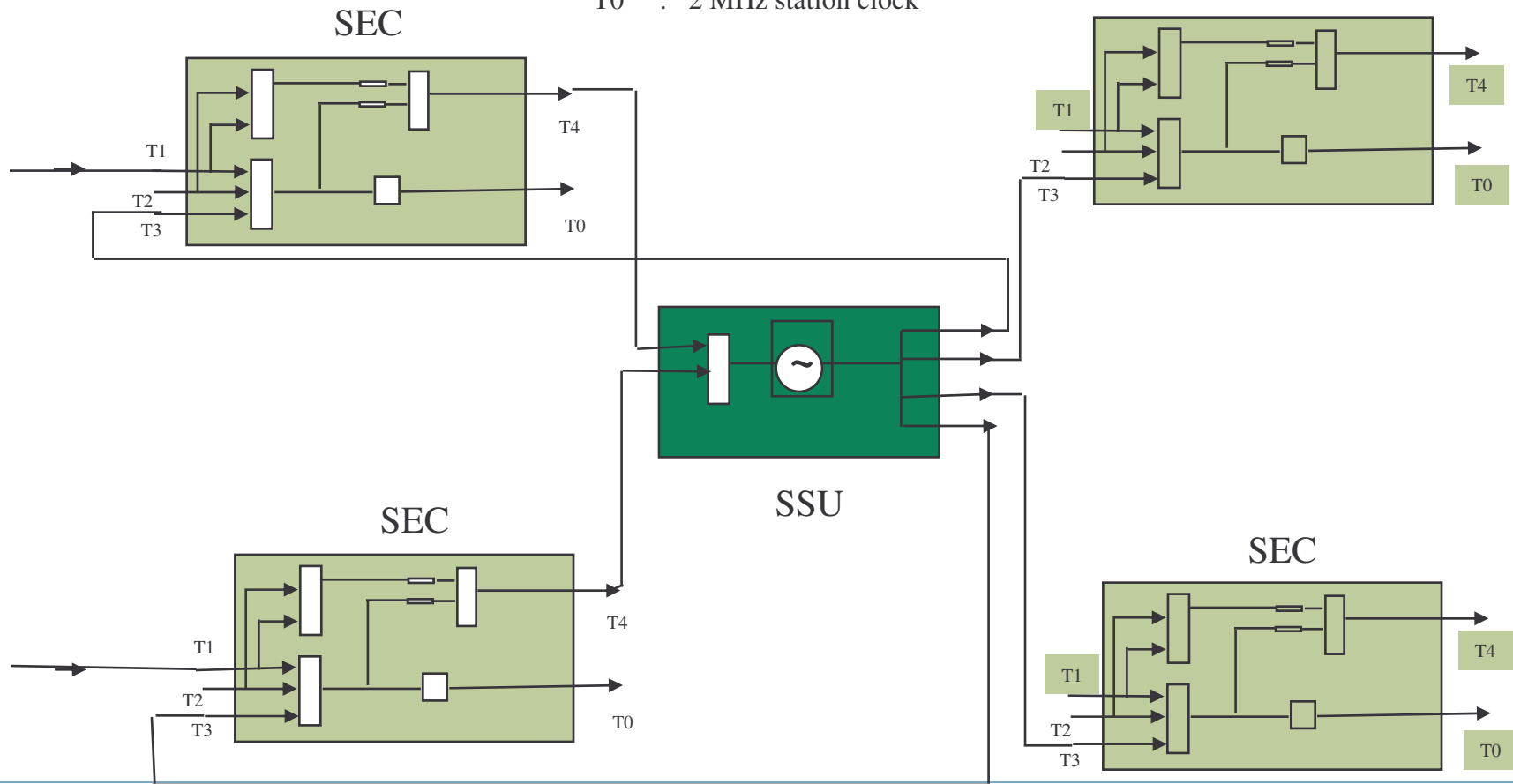
Using T0 output to send timing to the SSU presents 2 problems

- The SEC is not locked to the SSU if it sends timing to the SSU
- Getting timing from the SSU may cause SEC-SSU timing loop in case of STM-N LOS



Intra-node Architecture example

- T3/T4: 2MHz sync. signals
- T1 : 2 Mhz derived from STM-N
- T2 : 2 MHz derived from 2 Mbit/s
- T0 : 2 MHz station clock



SSM and ring architecture

> SSM definition

- A 4 bit code located in S1 byte of STM-N frame
- Indicates the Quality Level of the source of synchronization



>SSM application

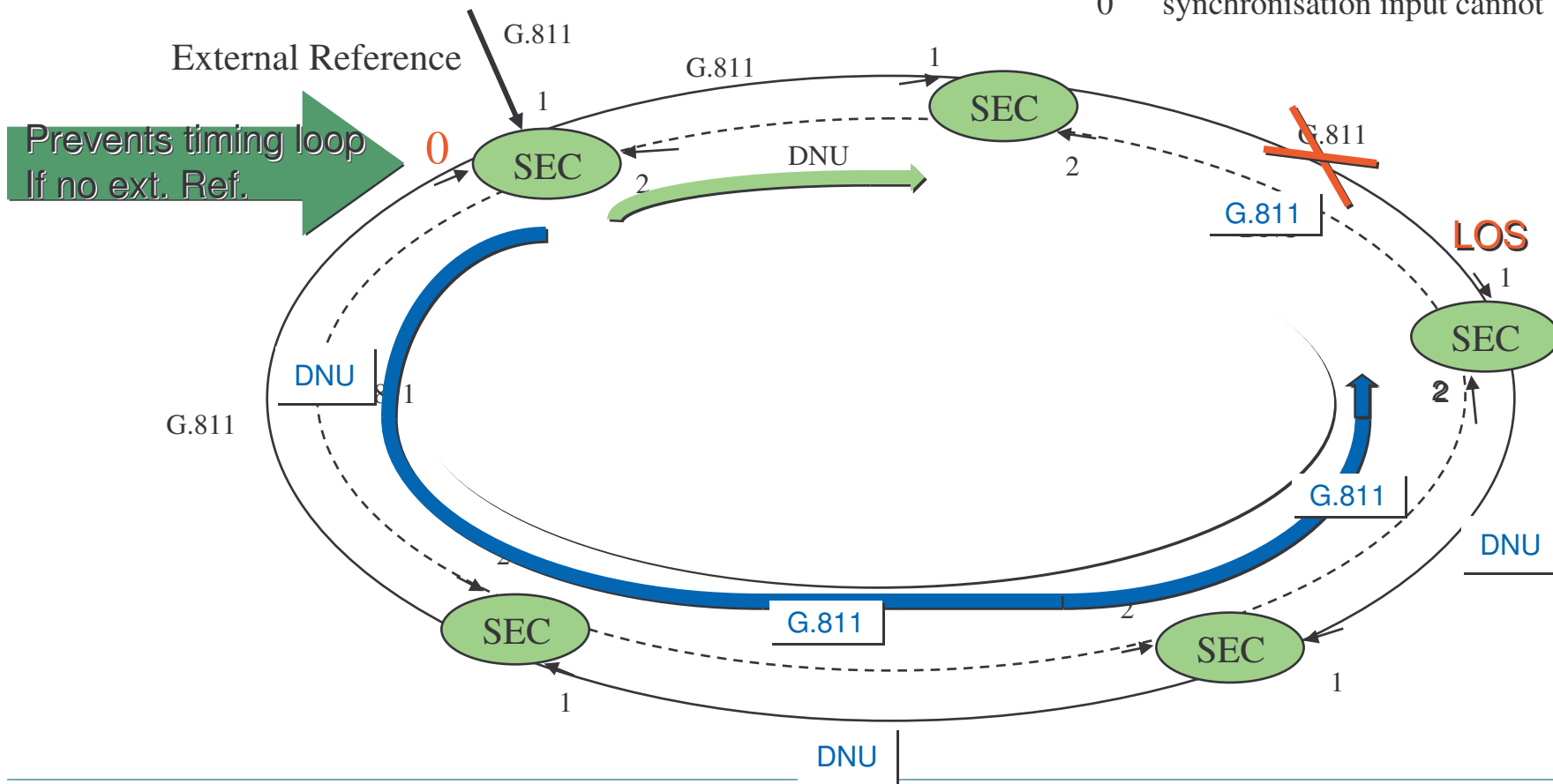
- Prevent timing loops
 - In linear chains and rings
 - In any combination of them
 - In meshed networks with some restrictions
- Helps in desynchronization detection

SEC-SSU interworking via 2Mbit/s

- > The standards, ETSI and ITU-T for SDH, did not agree on the general use of SSM between SEC and SSU due to:
 - the risk of timing loops in a mesh networks
 - some issues of delays between SEC and SSU switching times
 - The lack of a specific SSM code
- > As a consequence in SDH networks, the use of 2 Mbit/s signals is similar to the use of 2MHz signals between SEC and SSU.

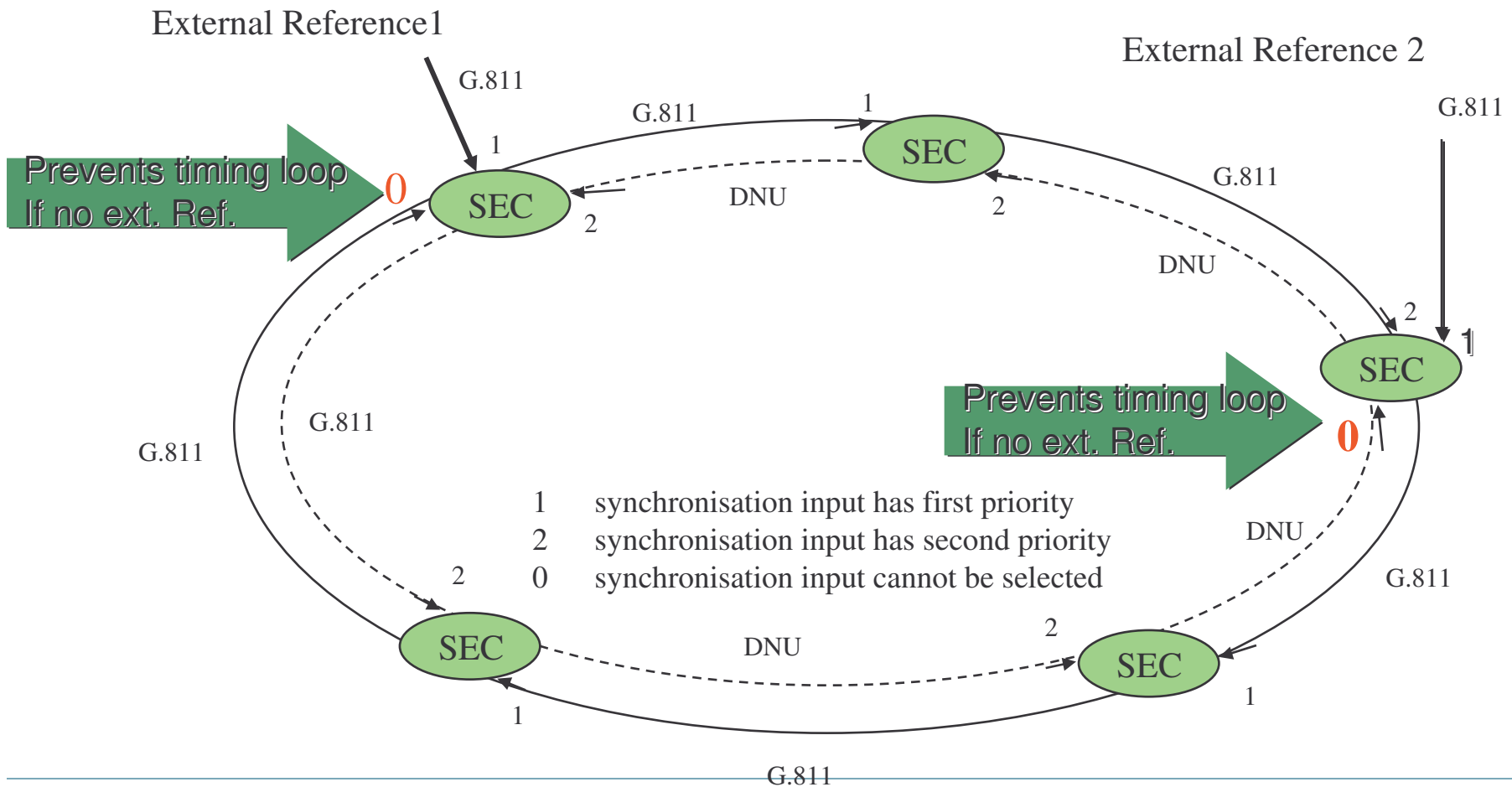
Use of SSM in rings with 2 external references

- 1 synchronisation input has first priority
- 2 synchronisation input has second priority
- 0 synchronisation input cannot be selected



Use of SSM in rings with 2 external references

- > Freeze 2 inputs of Nes with external reference

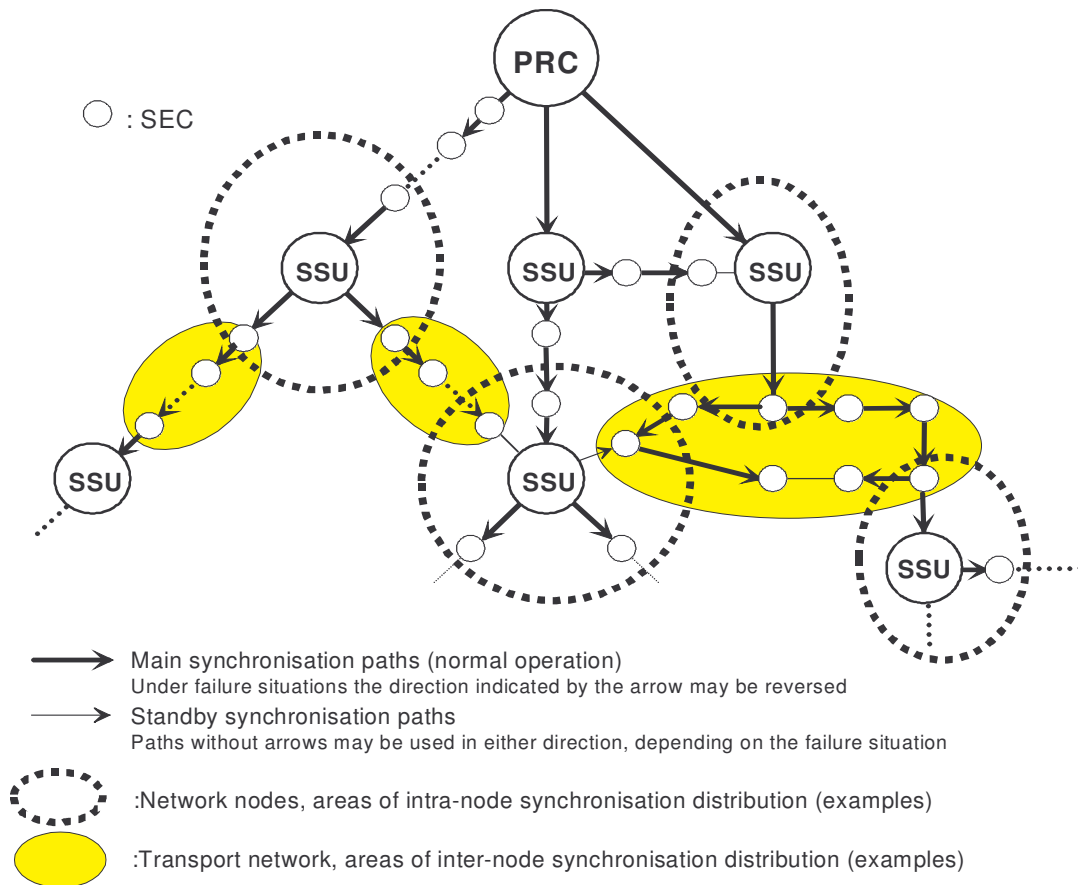


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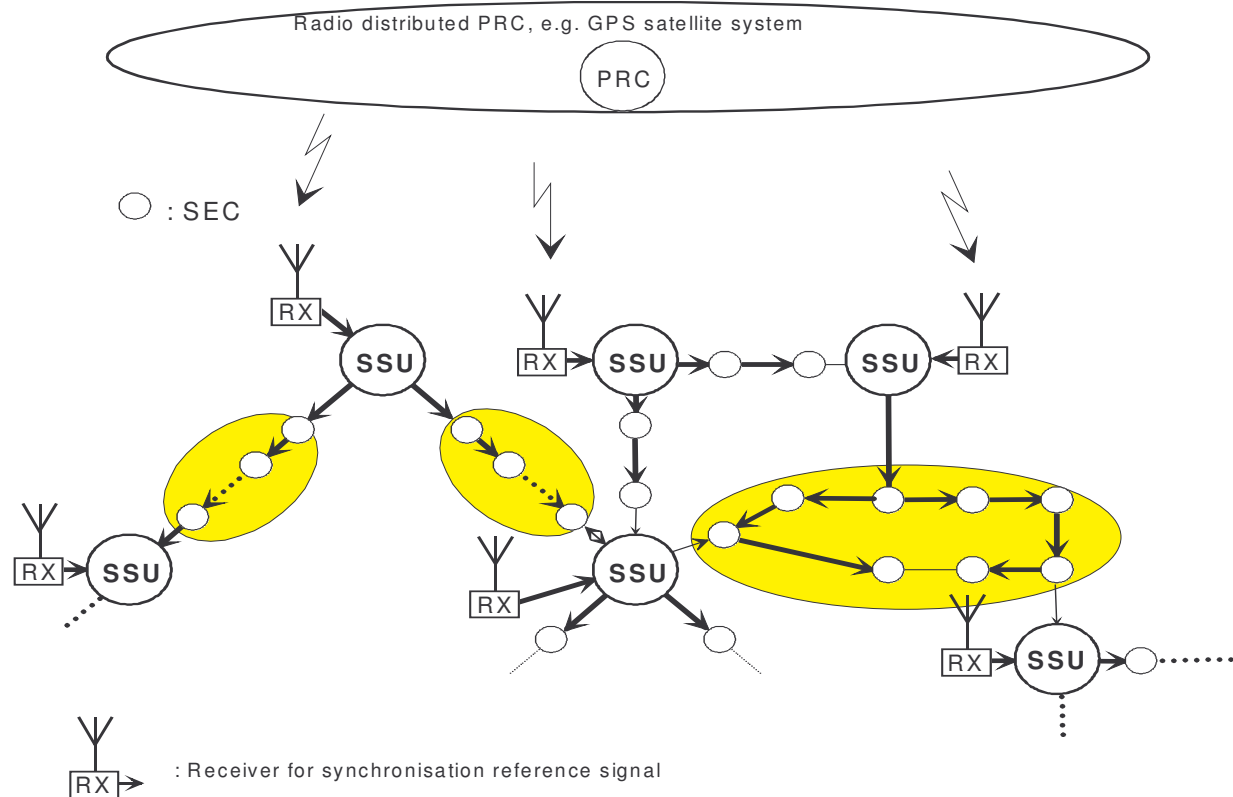
Hierarchical Master-slave solutions

- Easy and robust architecture, no timing loop
- May lead to long chains of clocks



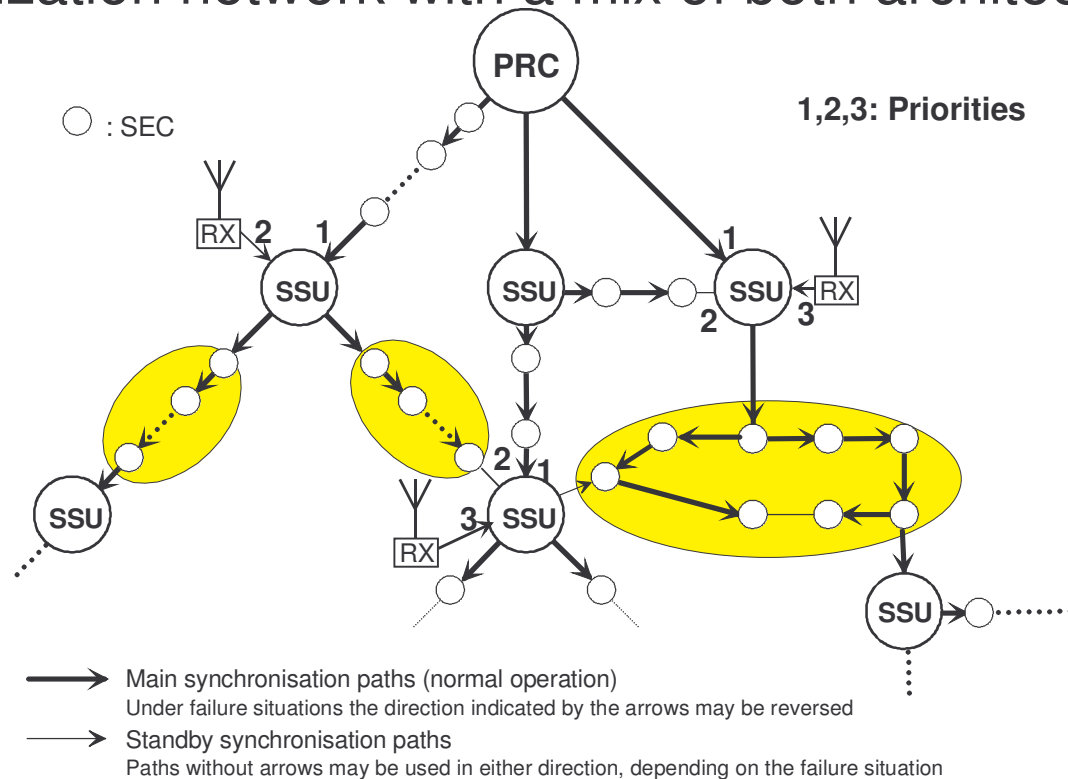
Distributed architecture

- > Example with use of GPS receivers
 - Short chain of clocks
 - High number of GPS receivers



Hybrid solutions

- > Each of the 2 architectures, centralised and distributed has its own drawbacks, and most operators are optimising their synchronization network with a mix of both architectures.



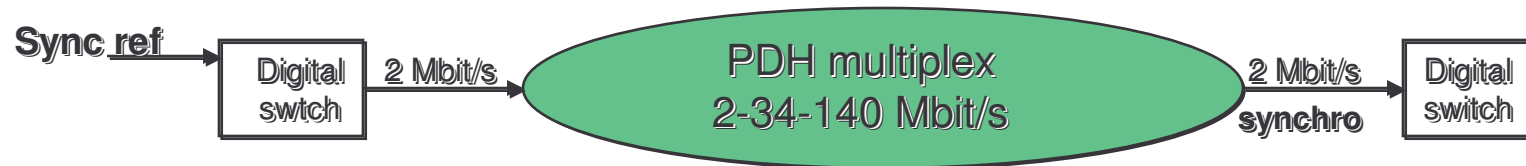
Note: It is possible to use GPS as priority 1 to shorten the synchronization chains

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Synchronisation of the E1 layer: the issue

- Before the introduction of SDH the E1 layer was synchronized via PABX which generate the 2 Mbit/s signals . These PABX were using the E1 layer to be synchronized



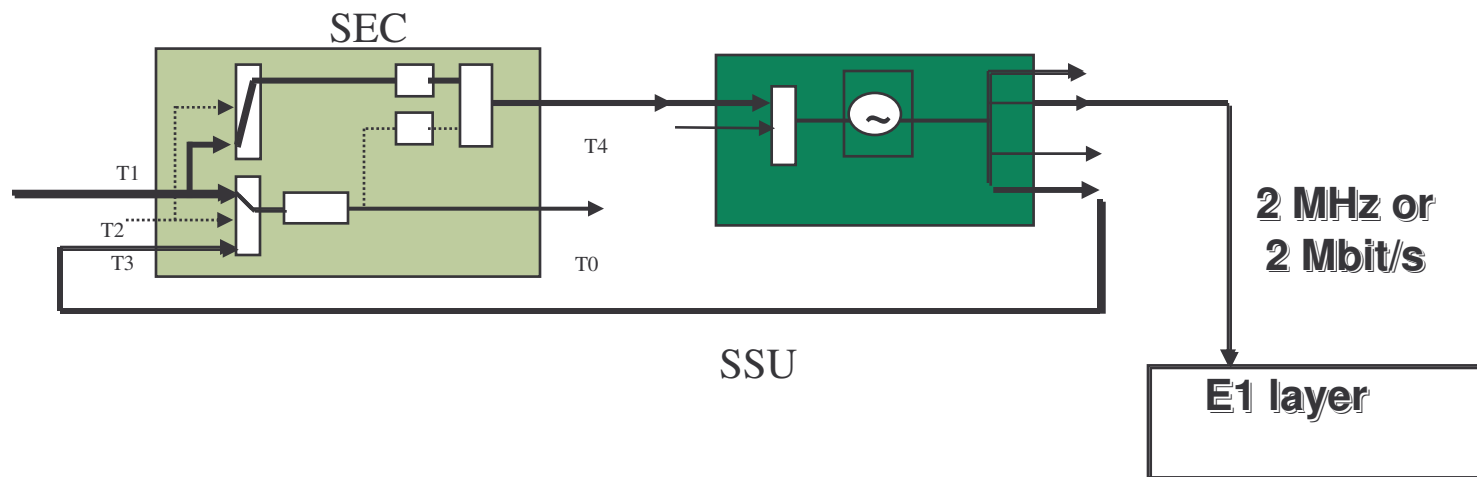
•SDH is now the sync layer

- E1 is floating within the SDH frame through an asynchronous mapping (Synchronous mapping has not been widely deployed)
- E1 is inappropriate to transport synchronization due to VC12 PJE



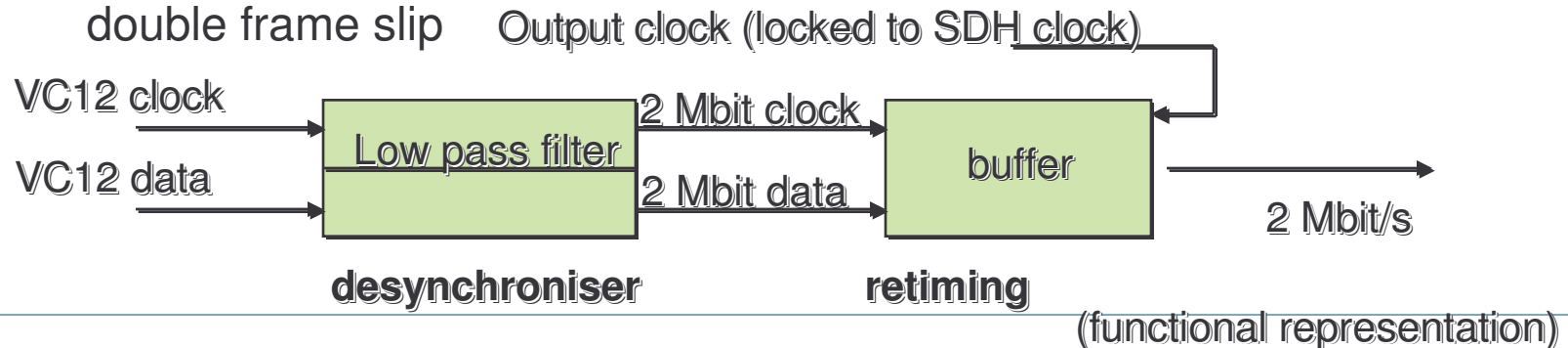
Synchronisation of the E1 layer: solutions

- The new synchronization layer being the SDH now, this layer is used to deliver timing to the digital switch
 - This is done by using the synchronization output, 2 MHz or 2 Mbit/s, of the SDH equipment which is derived from an STM-N signal
 - This may be done via an SSU, or not, depending on the quality of the digital switch clock



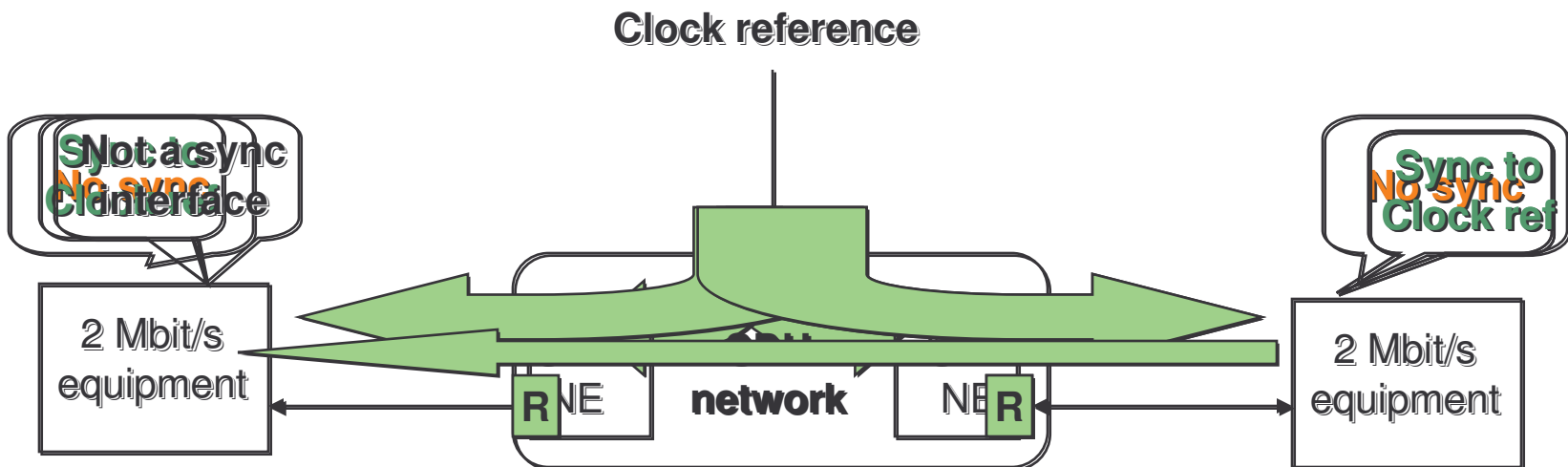
Synchronisation of the E1 layer: SDH NE retiming

- Another solution is to use a retiming 2 Mbit/s port in the SDH NE
- The retiming function is basically a buffer in which a 2 Mbit/s signal is entered with its own clock and which is extracted with the SDH clock of the SDH NE. Note that retiming is also implemented in some SSUs.
 - This allows to deliver a network synchronization quality to the 2 Mbit/s and get rid of phase jumps caused by VC12 PJE
 - This must be used only on synchronized 2 Mbit/s, otherwise bits will be periodically lost in the buffer
 - More generally, this function gives priority to timing and may alter the traffic
 - Several implementations exist: bit slip, byte slip, simple frame slip and double frame slip



Application of retiming

- > Application requiring synchronization



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Thank you