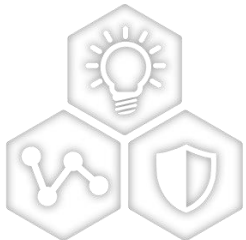


High Accuracy Optical Boundary Clocks



A Leading Provider of Smart, Connected and Secure Embedded Control Solutions



SMART | CONNECTED | SECURE

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How to Achieve Sub-Nanosecond PTP?

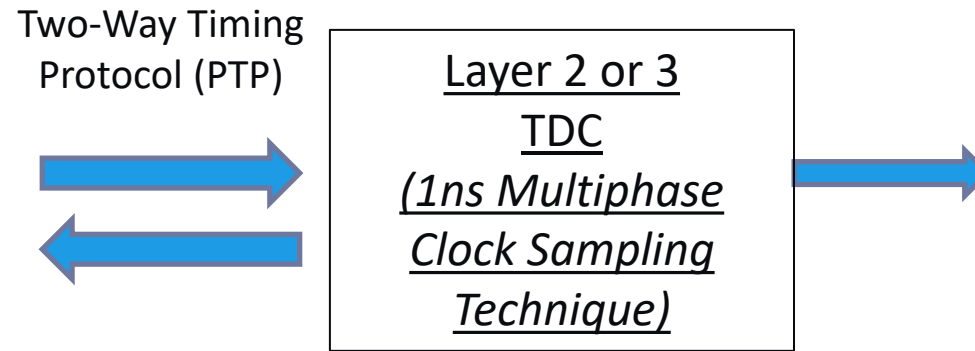
- Precision Timing Protocol is built on delay reciprocity
- Delay reciprocity simply means the delay in one direction is the same as in the other
- Optical transport without intervening processing nodes enables sub-nanosecond performance
- To realize optical accuracy the timestamping of timing packets is moved near the physical layer to minimize delay uncertainties
- This time stamping process (Time to Digital Conversion) is the key

What is Time-to-Digital Conversion?

- **Time-to-Digital Converter (TDC)** is a device for recognizing events and providing a digital representation of the time they occurred (Wikipedia)
- The 4 key timestamp events are at the heart of PTP (T1, T2, T3, T4)
- Primary objective is to achieve a TDC that does not limit underlying ultra-accurate optical time transfer

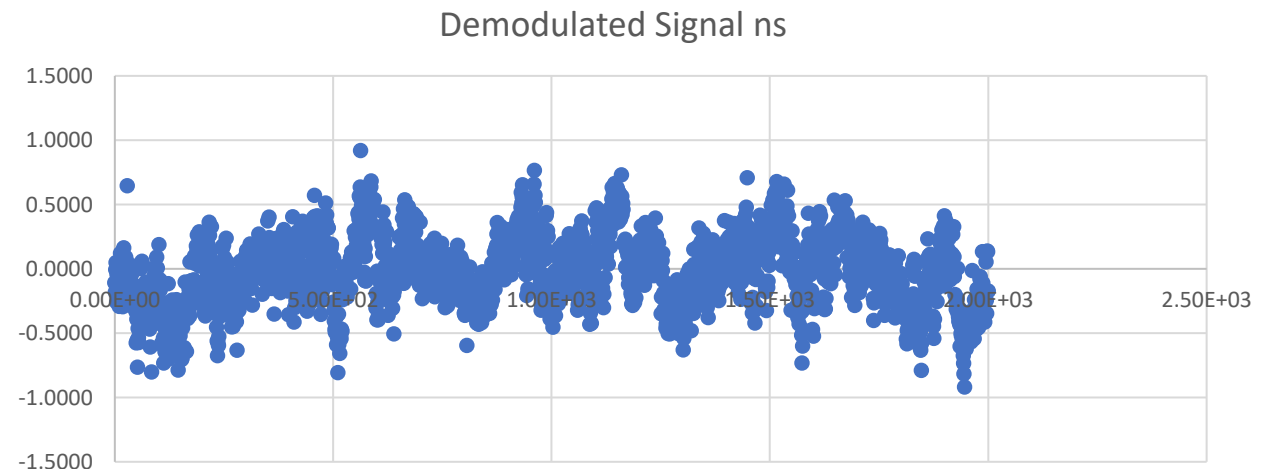
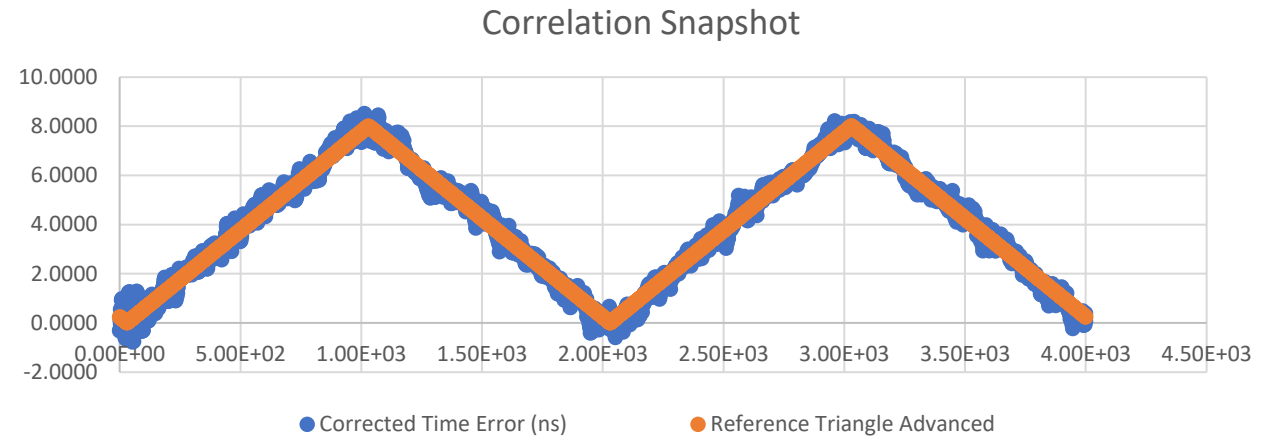
Time Digital Conversion in PTP Today

- TDC observes the local time of the arrival or launch of a key point in the PTP timing packet (Start Of Frame - SOF)
- Because of the serial to parallel conversion there is a 10-bit times on serial link ambiguity between the local receive 125MHz clock and the Start of Frame character
- Sub 8ns resolution required that this ambiguity be resolved
- With this correction we can consider the TDC timestamp as representing the timestamp of the SOF
- One technique to improve the resolution of the TDC is to operate effectively multiple TDC using for example 8 phases of the 125MHz clock to achieve a 1ns resolution



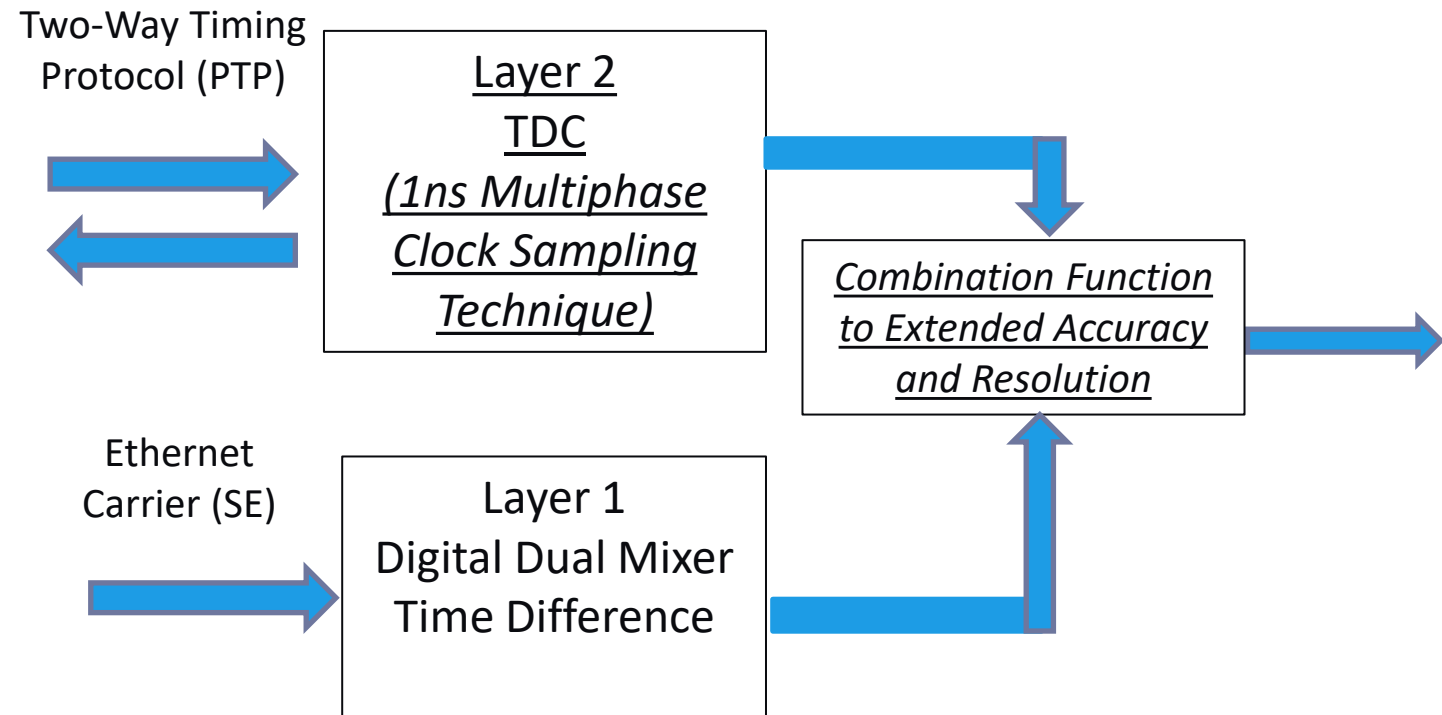
Multi-Phase TDC Characterization

- Multi-Phase TDC is sensitive to delay changes in the 8ns (125MHz related) range
- A proper implementation should achieve consistent results for all “fiber lengths”
- An 8ns delay sweep test is performed to characterize performance
- Residual demodulation error shows anticipated 1ns resolution errors
- Delay skews and meta-stable resolution effect add additional instabilities



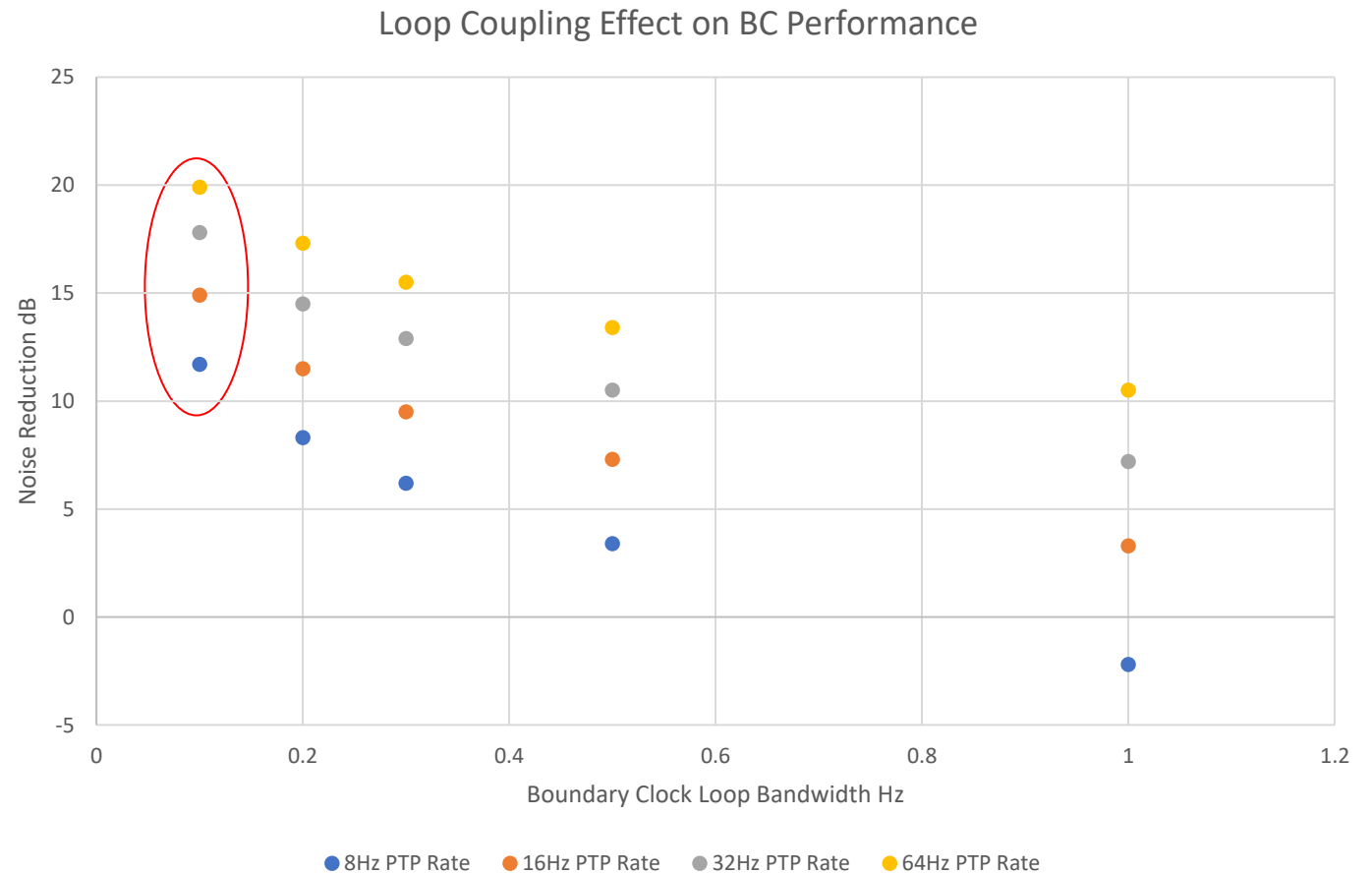
Time Digital Conversion Hybrid Approach H-TDC

- Sub-nanosecond high accuracy extension achieved with using synchronous ethernet
- Approach is analogous to the mature carrier phase enhancements used in GNSS
- Combination function performs cycle ambiguity resolution to generate a single extended resolution timestamp
- Integrity cross check of both paths ensures proper operation
- One time calibration is performed before field operation to ensure accurate timestamping and supports existing standard protocols (8275.1)
- Since the output is an ultra-accurate timestamp, existing analysis such as FPP can detect anomalies conditions



Optimized Loop Coupling

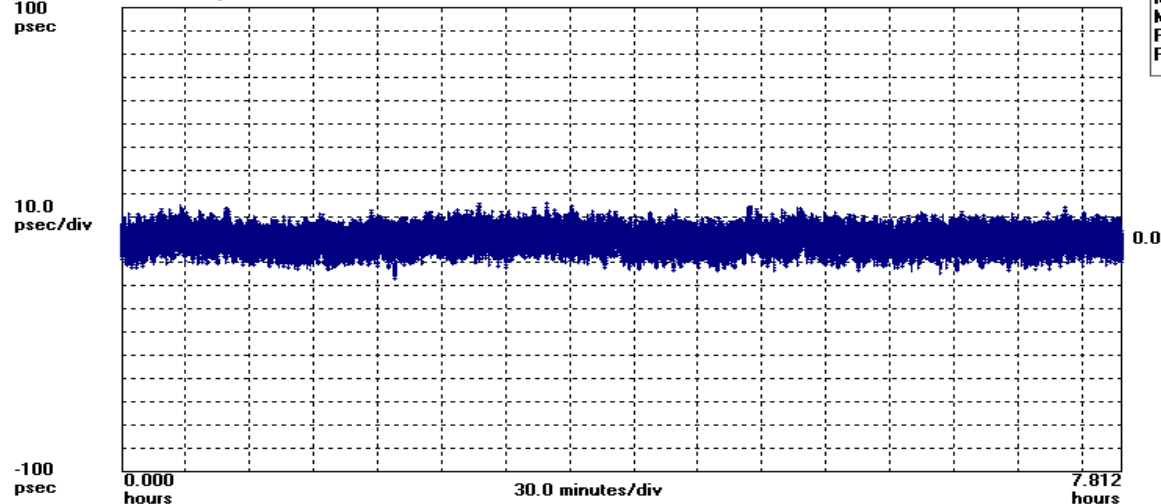
- Excellent oscillators and synthesizers permit filtering and even better time transfer
- The objective is to be “loosely coupled” to input to maximize transient rejection
- Graph shows additional reduction of TDC noise is achieved with optimal loop coupling
- Time Transfer Results shown with 0.1Hz loop coupling



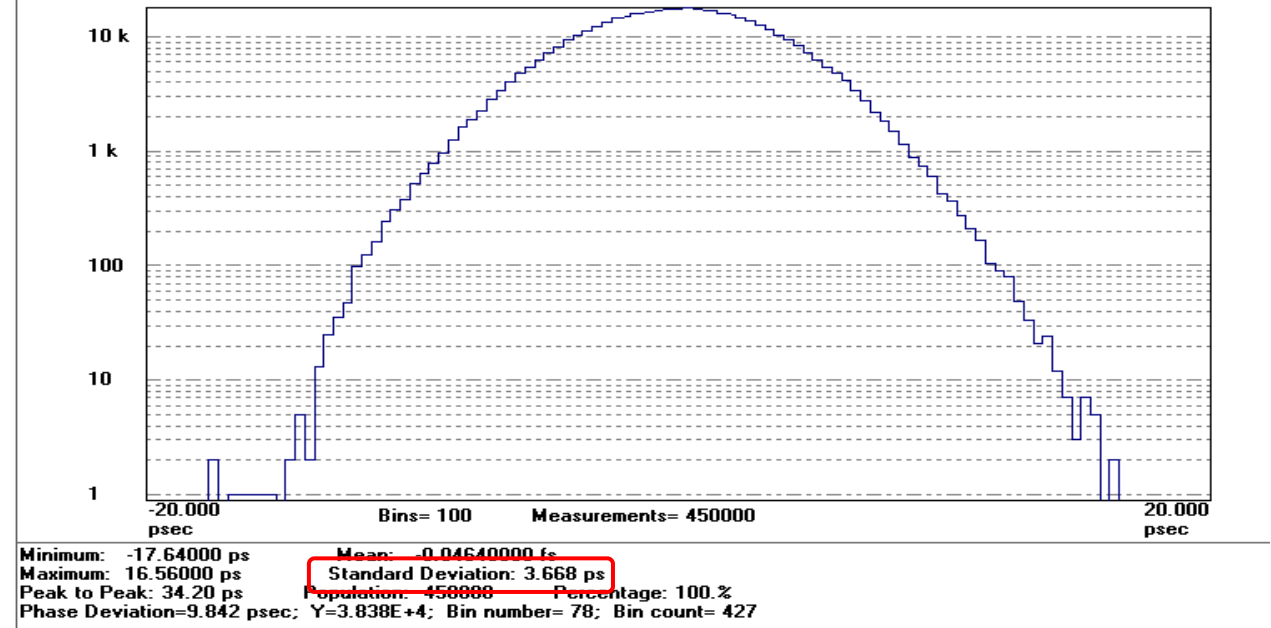
Hybrid TDC Time Transfer Baseline

- Two H-TDC configured units configured with common house reference as local oscillator
- Tested using standard G8275.1 protocol
- Short 2-meter optical cable used for baseline test
- Excellent single digit stability performance(<4ps Stdev)

Microchip TimeMonitor Analyzer
Microchip TimeMonitor Analyzer: 2021/10/11 05:09:04
2-Way H-TDC Time Transfer Performance 2 meter cable
Standard Deviation 3.62ps



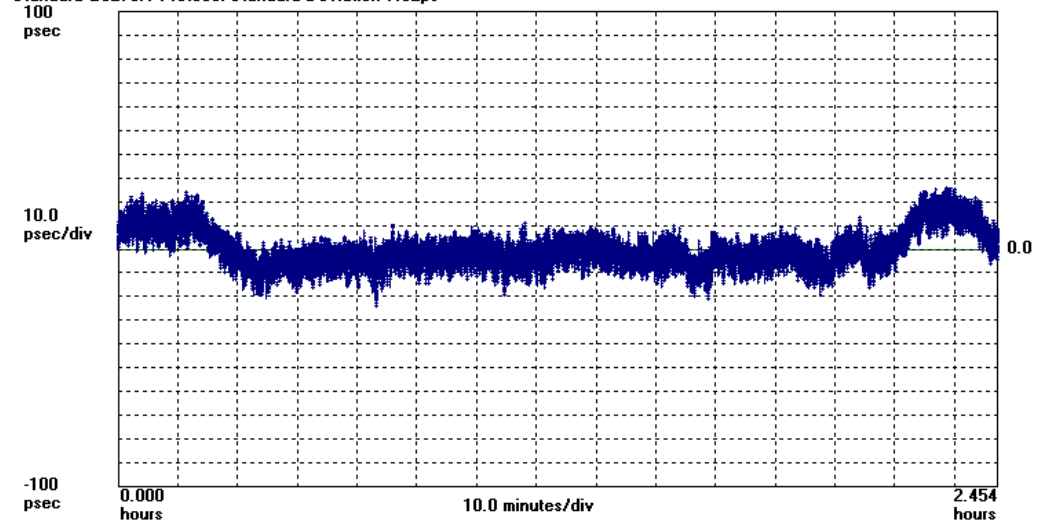
Microchip TimeMonitor Analyzer
Phase Deviation Histogram; Fs=16.00 Hz; Fo=10.00 MHz; 2021/10/11 05:40:13
2-Way H-TDC Time Transfer Baseline



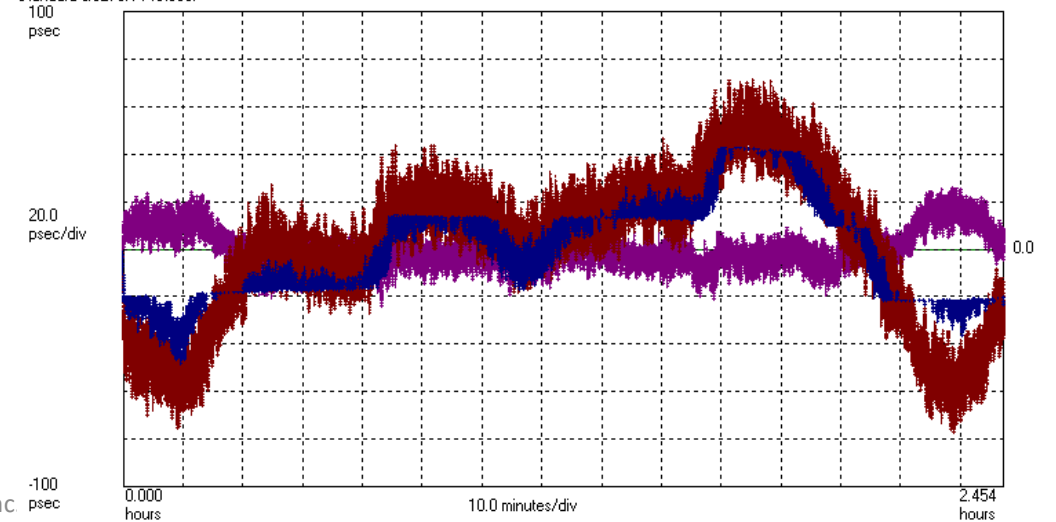
Hybrid TDC Time Transfer 60km Link

- Two H-TDC configured units configured with common house reference as local oscillator
- Tested using standard G8275.1 protocol
- 60km length (3 x 20km fiber spools)
- Common mode thermal delay observed in both directions effectively cancelled
- Time Transfer performance is maintained in single digits (<8ps Stdev)

Microchip TimeMonitor Analyzer
Microchip TimeMonitor Analyzer: 2021/10/11 05:22:04
Microchip H-TDC Two-Way Time Transfer 60km
Standard G8275.1 Protocol Standard Deviation 7.82ps

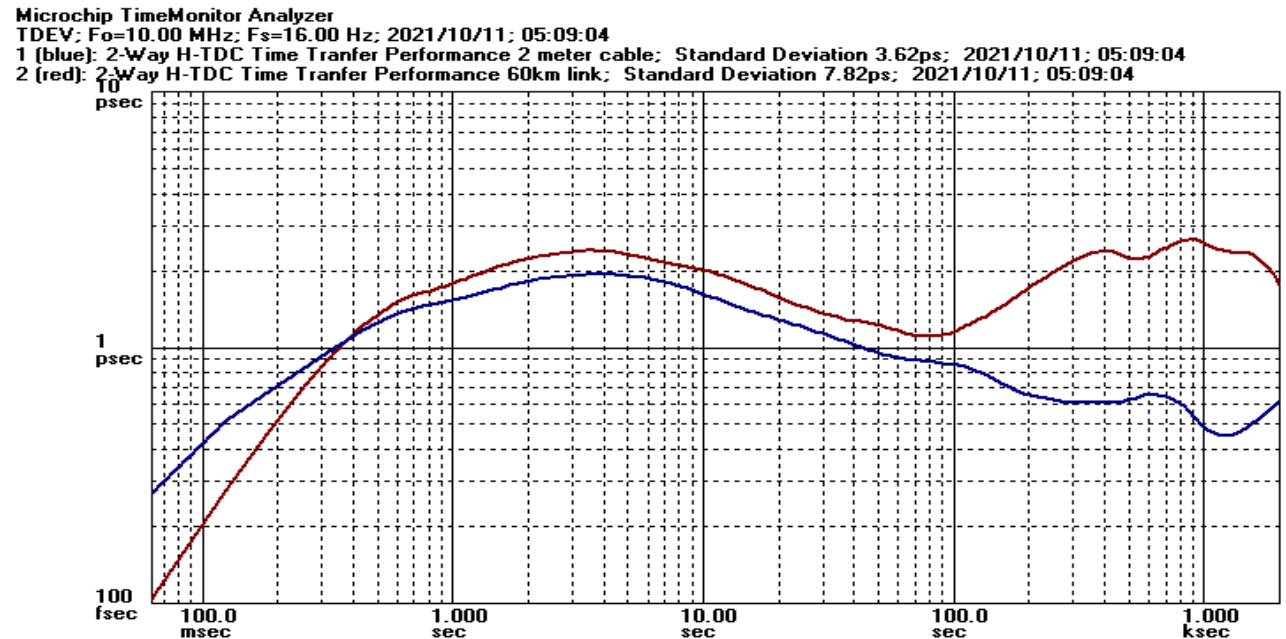


Microchip TimeMonitor Analyzer
Microchip hybrid TDC Time Transfer Overlay: 2021/10/08: 09:20:38
Red:Forward Blue: Reverse Magenta: Two Way Time Transfer
Standard G8275.1 Protocol



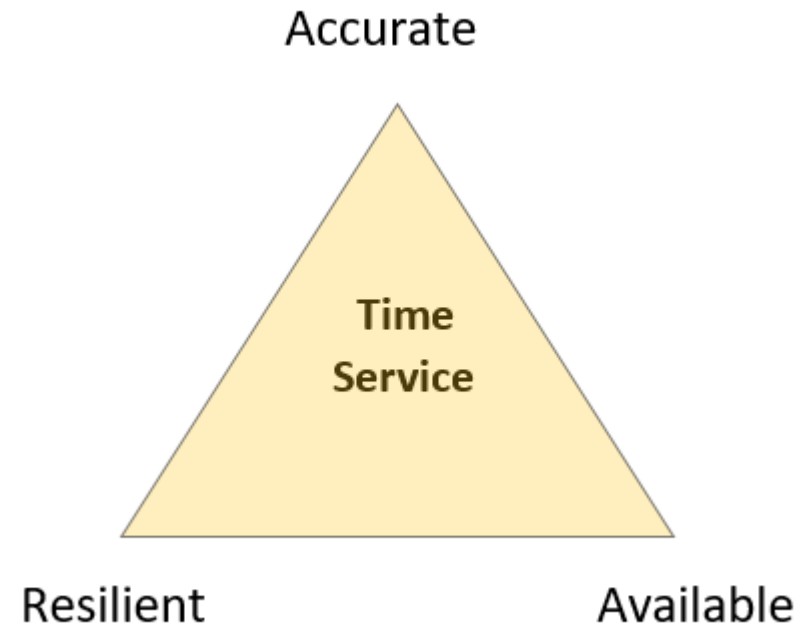
Hybrid TDC Time Transfer Stability

- Graph shows overlay TDEV stability for both baseline and 60km tests
- Stability performance in single digit ps over all observation windows
- 60Km results show modest increase in noise associated with optical link effects such as thermals and eye pattern degradation



Time Transfer more than Accuracy

- High **Accuracy** is not the whole story
- For most applications, there is a need to deliver time services in real time
- A complete system must address Resiliency and Availability
- **Resiliency** ensures system can tolerate real-world issues such as intentional or unintentional degradation of optical link or device
- **Availability** ensures that the system has adequate redundancies and backup to maintain high accuracy under failure and maintenance



Summary

- **Hybrid TDC achieves full single-digit picosecond optical time transfer performance**
- **Optical Boundary Clocks with Hybrid TDC synergistic with standards**
 - Sub-Nanosecond does not require new protocol standards BUT ...
 - H-TDC is interoperable with new high accuracy protocols
- **Optical Boundary Clocks need to address not just high accuracy but also resiliency and availability**

Thank You