

New Real Time Clock Combines Ensemble of Input Clocks and Provides a more Stable Output than Any of the Input Clocks

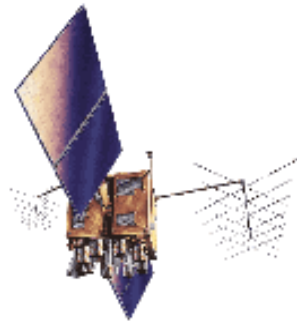
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Purpose of the Clock

- Is to provide a stable clock signal

based on

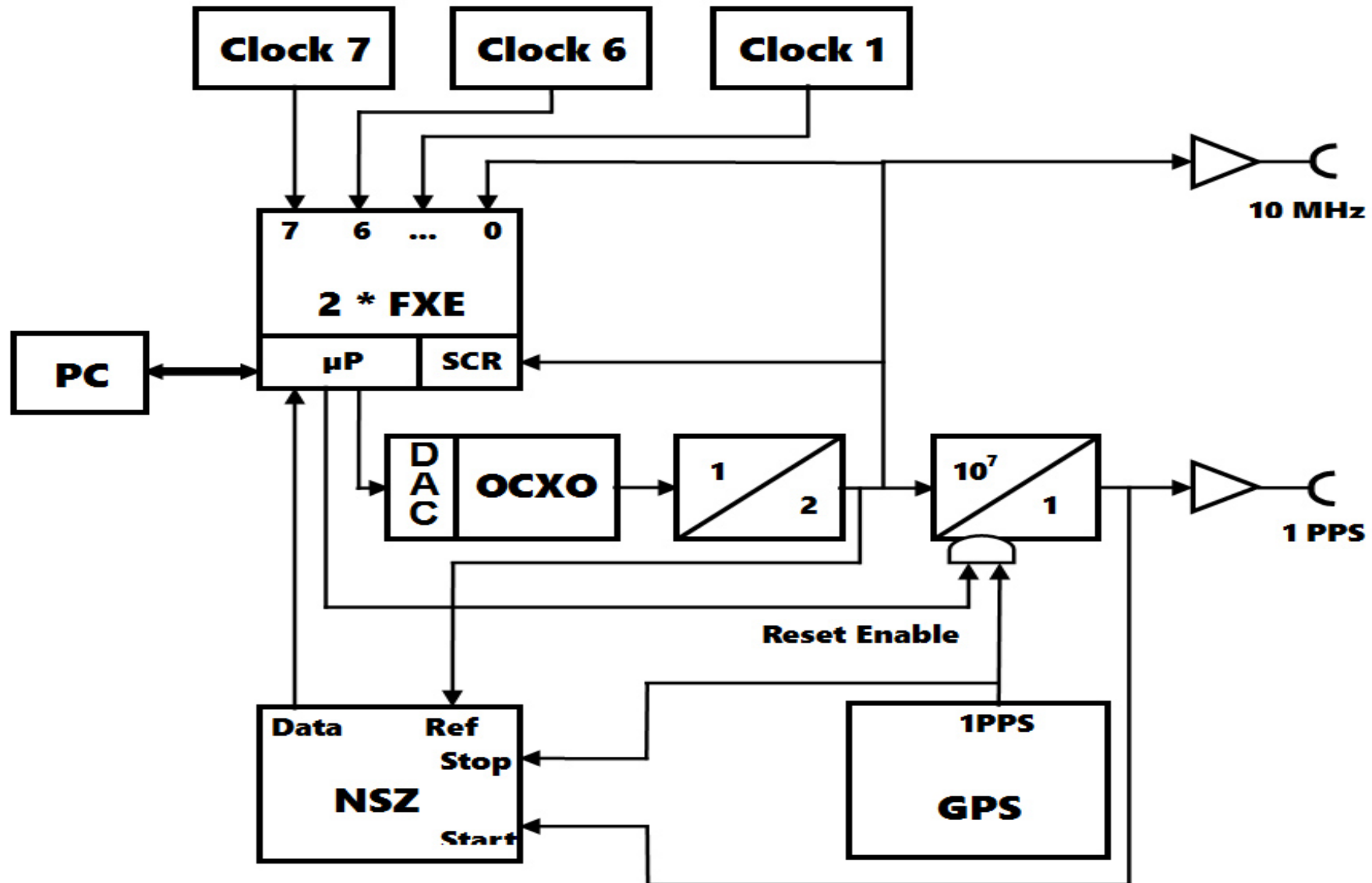
- short term frequency stability of the built-in OCXO
- the medium term frequency stability of a set of atomic clocks
- the long term timing accuracy of a GPS timing receiver

which will continue its phase track even if one or even a few of the contributing clocks fail.

Benefits of the Software Clock:

- Improved stability as compared to a single atomic clock due to ensemble averaging over a set of up to 7 clocks
- Automatic steering to UTC(GPS),
 - Additional phase and/or frequency steering on operator command,
- Continuous consistency check among the atomic clocks,
 - Robustness against clock failures,
- Easy clock maintenance without interruption of the Software Clock output signal.

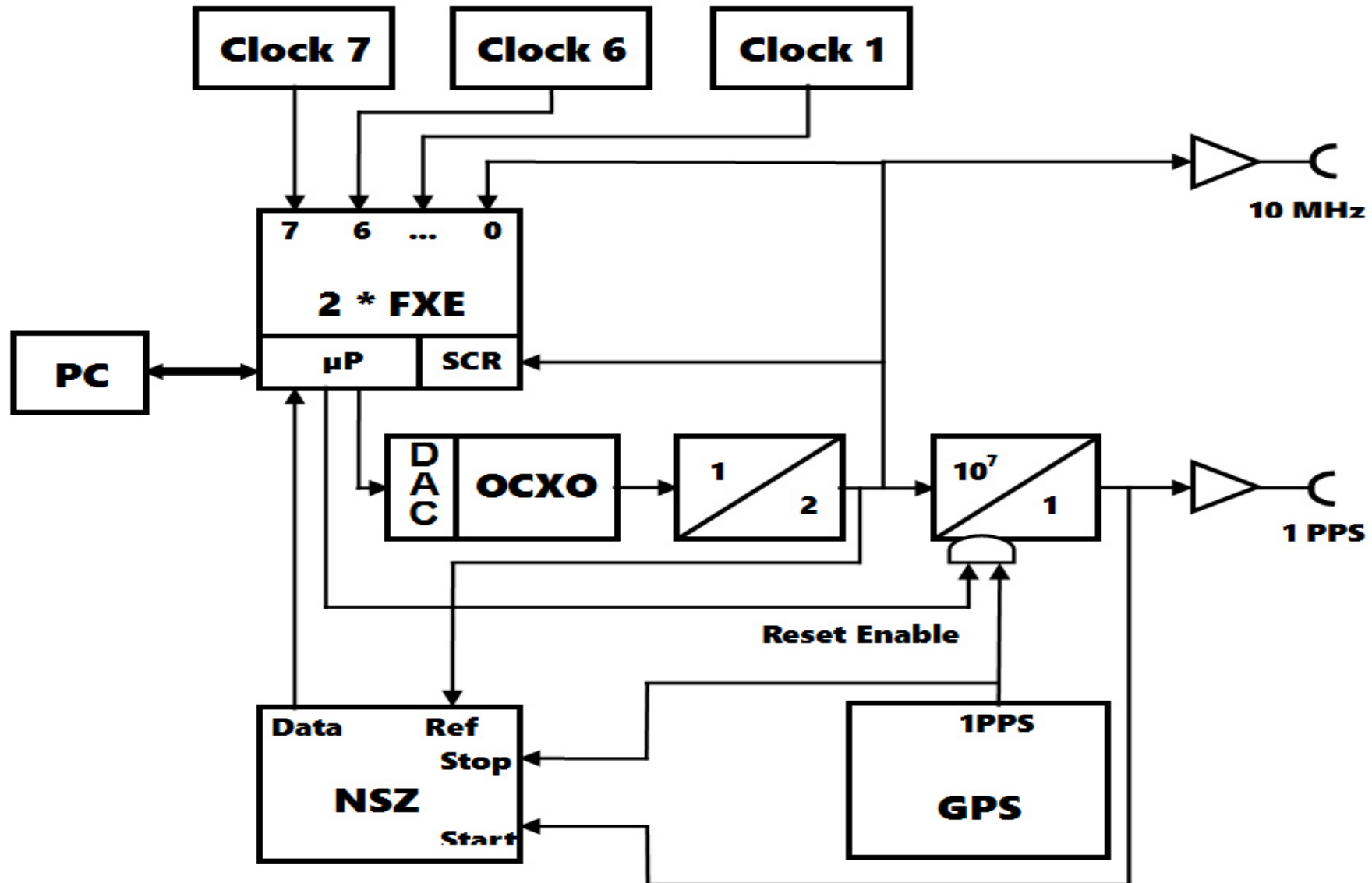
Block Diagram



Components

- A **clock generator board** generating (at least) 10MHz and a 1PPS from an OCXO
- Two **multi-channel phase meter boards** for up to 7 clock input channels
- A **time interval counter** for the 1PPS measurement of SWC time to GPS time,
- A power supply.

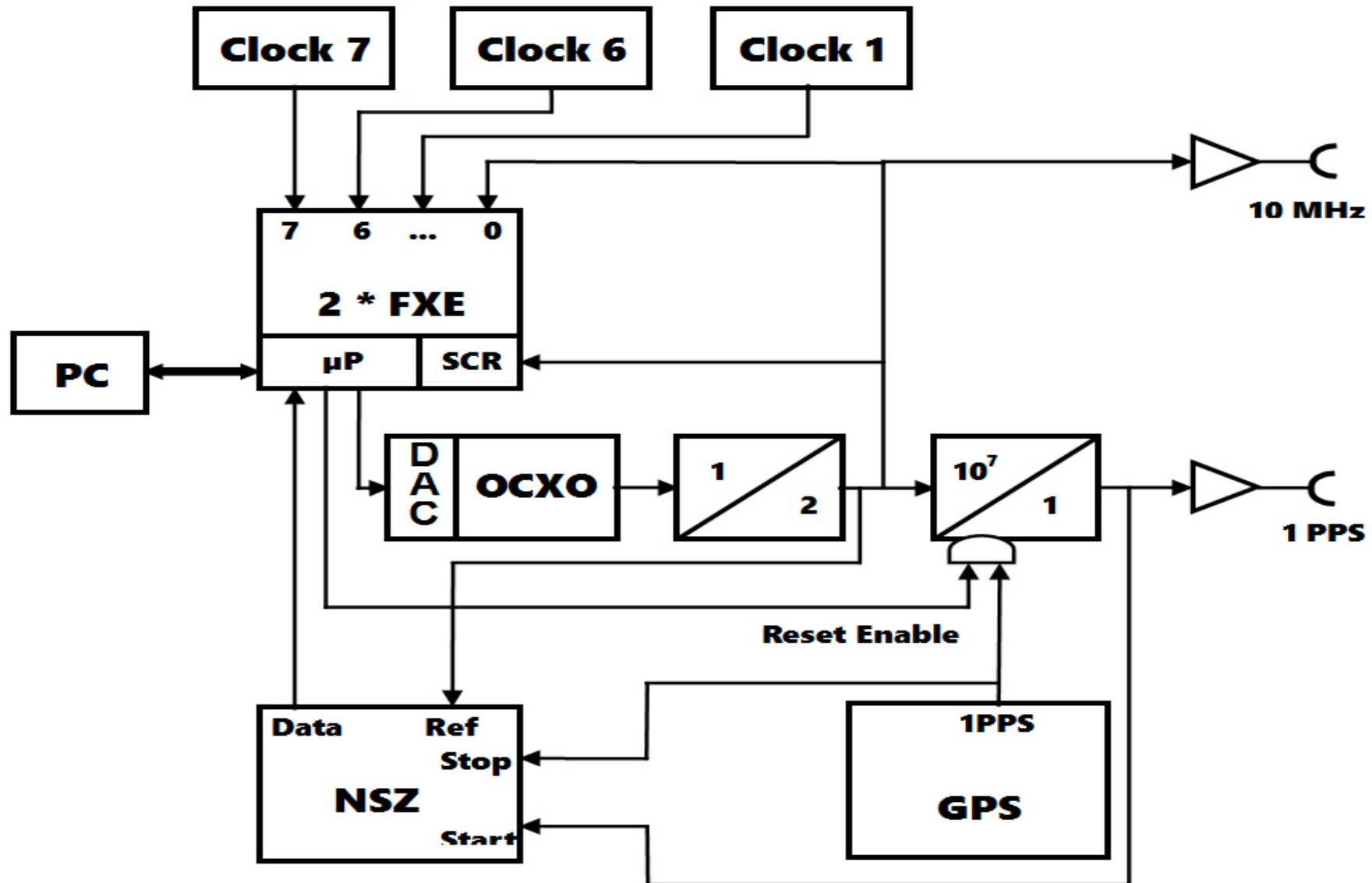
Block Diagram



Time Interval Counter

- The **Time Interval Counter** (NSZ) measures the time from the rising edge of a start pulse to the rising edge of a stop pulse.
- The time scale is defined by a 10MHz reference clock signal.
- The numerical resolution is 50ps (1/2000th of a reference clock period), and the accuracy is appr. 150ps.
- The measurement result is serially transmitted to a microprocessor.
- The FXE microprocessor accepts the NSZ data and forwards them to the PC.

Block Diagram



Software Clock - 1

- Contains 5MHz high stability OCXO and a high resolution (24bit) DAC for frequency tuning
- a 10MHz oscillator phase locked to the 5MHz
- a resettable 1PPS divider
- optionally a 100MHz oscillator phase locked to the 5MHz.
- Key parameters of the OCXO (5 MHz) used are:
 - Frequency stability vs. temperature changes pk-pk: $<5E-10$
 - Aging: $<5E-10$ per day / $<5E-8$ per year
 - Allan Deviation: $<3.5E-13$ @ 1s & 10s

Software Clock - 2

- Guarantee strict monotonicity and a reasonable linearity are crucial within a closed phase locked loop
- high resolution **DAC** is built using a guaranteed monotonic 16 bit DAC
- being updated at a rate of 1kHz with a sequence of 16-bit-words, the average of which represents the 24-bit-value to be converted.
- To produce that average, the output voltage generated by the DAC is RC filtered with a time constant of about 100 ms, which has the additional benefit of reducing the noise on the OCXO tuning voltage.

Software Clock - 3

- The frequency doubler is made up of a 10 MHz quartz crystal oscillator
 - - phase locked to the 5 MHz input.
 - - generates a square wave output signal to assure a well-defined phase time for the phase lock.
 - - two-stage filter extracts a sine wave signal, which is distributed to the other elements on the board.

Synchronous Phase Meter Boards

- Two multi-channel **Synchronous Phase Meter** boards

- are concatenated to provide

- **simultaneous phase measurements**

- from 8 clock sources: the 10MHz clock signal from the

- SWC board (channel 0) and

- up to 7 external atomic clocks (channels 1..7).

- An (optional) **Scrambler** is available to assure highest performance – it reduces the channel cross talk to less than 10ps.

Key Features

■ Key features of FXE relevant to this application are:

■ - Internal measurement rate: 1 kHz

■ - Uncertainty of raw measurement: 15 ps

■ - Report of phase difference averages: every 100 ms

■ - Uncertainty of reported phase differences: 1.5 ps

■ - Numerical resolution of reported phase differences: 30 fs

Software - 1

- The 10 MHz frequency doubled OCXO signal is internally delivered to the phase meter both as the reference signal and as input to its channel 0.
- The inputs to channels 1..7 are connected to front panel connectors to accept 5 MHz or 10 MHz clock signals (phase readings from 5 MHz input signals will automatically be doubled by the software to be immediately comparable to readings resulting from 10 MHz input signals).
- Every 100 ms the FXE reports the phase difference of each of the seven clock input channels to channel 0 (i.e. the phase difference between each of the atomic clocks and the OCXO).
- In detail, reported phase differences are the average of 100 measurements taken at 1ms intervals. Additionally, a continuously incrementing 'number of measurement' is included, which serves as a time stamp within the PC data processing:

Software - 2

- Software controls OCXO that it generates a smooth and stable time scale based
 - - on the intrinsic OCXO stability in short term
 - - on the contributing clocks' stability in medium term
 - - and governed by the 1PPS from a GPS receiver in long term.
 - - Basically the OCXO's phase is locked to the weighted mean of the contributing atomic clocks.
 - - Without inclusion of GPS/GNSS 1pps both phase and frequency would be arbitrary

Software - 3

- To provide long-term absolute timing accuracy, a slowly varying time offset resulting from the 1PPS TIC measurements (with a time constant of typically several days) is added to the weighted mean of clock phase offsets.
- A manually entered time and/or frequency offset may be added to the TIC results to compensate for cable delays etc.
- An initial 'learning' session is required during which all contributing clocks must be OK for the SWC to start properly
- The parameters for linear fits of each clocks' phase difference to the OCXO's phase versus time are being established for the first time. Actually it is during this initial learning session that the future phase and frequency of the SWC time are being established.

Software - 4

- If one of the clocks exhibits a phase jump or a change in frequency large enough to be observable its fit parameters will no longer be updated, but instead will be frozen.
- The phase control loop will no longer use that clock's actual (faulty) measured phase difference data, but instead will replace them by the value estimated from the frozen linear fit parameters.
- Thus the time evolution will continue to follow the same phase track as it did before the fault; the time scale realized by the SWC will continue without a change in phase or frequency.
- The faulty clock's phase will continue to be measured against the OCXO phase, and the data will continue to be checked for phase steps and for Allan deviation. If, after a reasonable time of observation, no further anomalies have been observed, the clock is considered healthy again and a new initial set of linear fit parameters is determined.

Clock Management - 1

The management of the clocks is described by the combination of three attributes: Mode, Status and Health.

MODE takes one of three values, **include** , **monitor** or **ignore** .

'**include**' means that the clock is contributing to the Ensemble average - either (if it is considered healthy) with its latest measurement results, or otherwise with data estimated from the fit.

'**monitor**' describes the mode where a clock's measurements are continuously evaluated to check for faults and to update the fit in regular intervals, but that clock does not contribute to the ensemble time, and hence has no influence on the OCXO control.

'**ignore**' means that data for that clock are not being considered at all.

Clock Management - 2

Status is one of **known**, **learning**, or **initial**

„known“ means the respective clock has been measured sufficient long time without a fault, phase and frequency offset could be determined from past measurement data.

A clock that has not been continuously measured or has shown a fault is put into status „learning“.

Right after the start of the software all clocks are assigned the status „initial“.

Clock Management - 3

Health always has three values **good**, **dubious** or **faulty**.

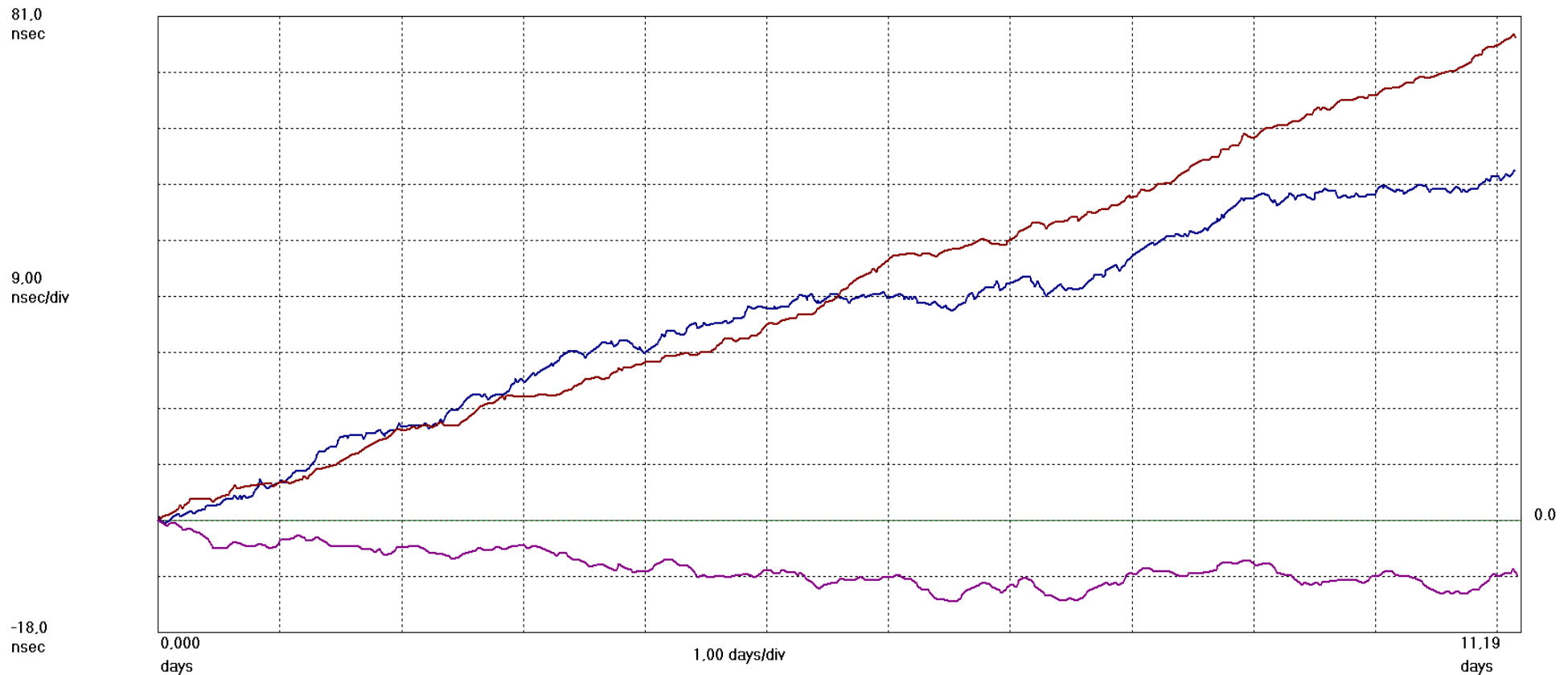
Normally the health value of contributing clocks will be „good“, the fit parameters will be updated regularly and that clock will contribute to the ensemble time.

At the start of the software the status of all clocks is set to „dubious“. This coincides with the status „initial“ and is valid only right after the start of the software.

If either a phase step or a change of frequency relative to the ensemble time is observed the health will change to „faulty“, the updating fit will be suspended and the last good fit parameters will be used.

2 Free Running CS-Clocks Versus RTC Output

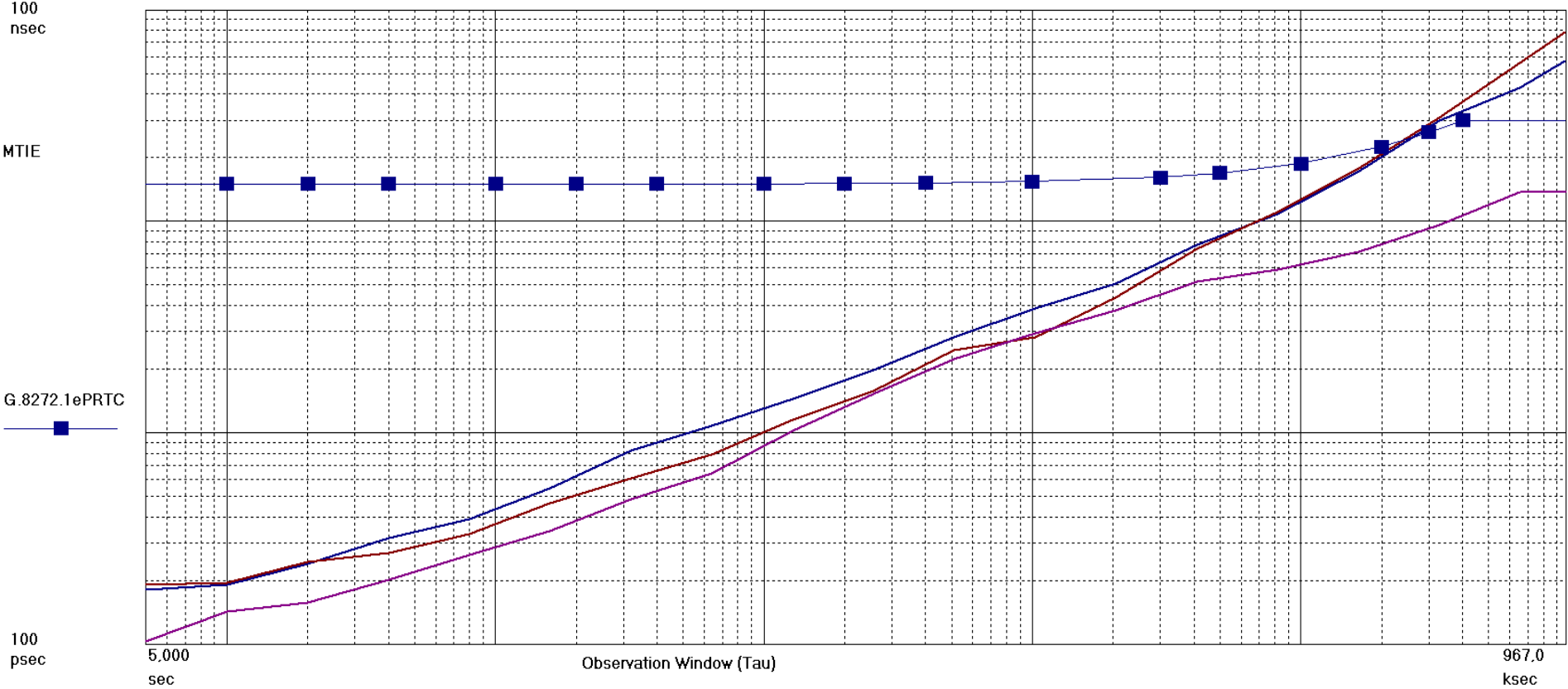
1 (blue): Agilent 53220A; Test: 3; 10MHz_5071A-C8; 10MHz.UTC; Samples: 193320; Gate: 5 s; Ref ch2: 10.00 MHz; TI/Time Data Only; TI 1->2: 10MHz_5071A-C8-UTC; 2015.06.25; 13:11:31
2 (red): Agilent 53220A; Test: 4; 10MHz_5071A-C3; 10MHz.UTC; Samples: 193320; Gate: 5 s; Ref ch2: 10.00 MHz; TI/Time Data Only; TI 1->2: 10MHz_5071A-C3-UTC; 2015.06.25; 13:11:31
3 (magenta): Agilent 53220A; Test: 5; 1pps_K&K; 1pps.UTC; Samples: 193401; Gate: 5 s; Ref ch2: 1.000 Hz; TI/Time Data Only; TI 1->2: 1pps_K&K-UTC; 2015.06.25; 13:11:31



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Same Cs - Clocks - MTIE

1 (blue): Agilent 53220A; Test: 3; 10MHz_5071A-C8; 10MHz.UTC; Samples: 193320; Gate: 5 s; Ref ch2: 10.00 MHz; TI/Time Data Only; TI 1->2; 10MHz_5071A-C8-UTC; 2015.06.25; 13:11:31
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Linear Fit of 3 Cs and 2 Maser



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