

Standardizing clocks

Silvana Rodrigues, System Engineering, IDT, <u>silvana.rodrigues@idt.com</u> ITSF 2014

4 - 6 November, 2014, Budapest, Hungary





Agenda

- ITU-T Clock Hierarchy (G.803)
- Equipment Clocks
- Clocks for Frequency
- G.8263
- Clocks for Phase/Time
- G.8272
- G.8273.2
- Summary



ITU-T Clock Hierarchy (G.803)

PRC – Primary Reference Clock Highest quality clocks : Frequency accuracy < 10⁻¹¹

Defined in ITU-T recommendation G.811

SEC – SDH Equipment clock

Defined in ITU-T recommendation G.813
 Used in Routers, ADMs, MSPPs etc.

SSU – Synchronization Supply Unit (high quality clocks)

Defined in ITU-T recommendation G.812

Clocks are based on Phase Lock Loop concept

- ITU-T G.810 defines the clock modes of operation
- As clocks are cascaded, it is important to limit noise accumulation
- Proper bandwidth and gain peaking are important (wander transfer)
- Performance under failure conditions are also very important to be specified (e.g., holdover, transient response)

SDH Synchronization chain is defined in ITU-T Rec. G.803

- Consists of 1 PRC followed by 20 SECs, followed by SSU
- The maximum number of SSUs is 10
- The maximum number of clocks is 60









Equipment Clocks

Clocks for Frequency

- > G.8262 Timing characteristics of Synchronous Ethernet Equipment slave clock (EEC)
- > G.8263 Timing Characteristics of Packet based Equipment Clocks (PEC) and Packet based Service Clocks (PSC)
- > G.8266 Timing characteristics of telecom grandmaster clocks for frequency synchronization (under development)

Clocks for Time/Phase

- ➤ G.8272 Primary Reference Timing Clock (PRTC) specification
- > G.8273 Clock General Requirements
- ➤ G.8273.1 Telecom Grand Master specification (under development)
- ➤ G.8273.2 Telecom Boundary Clock specification
- > G.8273.3 Telecom Transparent Clock specification (under development)
- > G.8273.4 Timing characteristics of assisted partial timing support slave clocks (under development)





Equipment Clocks

Clocks for Frequency

- G.8262 Timing characteristics of Synchronous Ethernet Equipment slave clock (EEC)
 (Consented)
- > G.8263 Timing Characteristics of Packet based Equipment Clocks (PEC) and Packet based Service Clocks (PSC)
- G.8266 Timing characteristics of telecom grandmaster clocks for frequency synchronization

Clocks for Time/Phase

- G.8272 Primary Reference Timing Clock (PRTC) specification (Consented)
- G.8273 Clock General Requirements (Consented)
- ➤ G.8273.1 Telecom Grand Master specification
- ➤ G.8273.2 Telecom Boundary Clock specification (Consented)
- ➤ G.8273.3 Telecom Transparent Clock specification
- > G.8273.4 Timing characteristics of assisted partial timing support slave clocks





G.8261.1 Hypothetical Reference Model 1 (HRM-1)

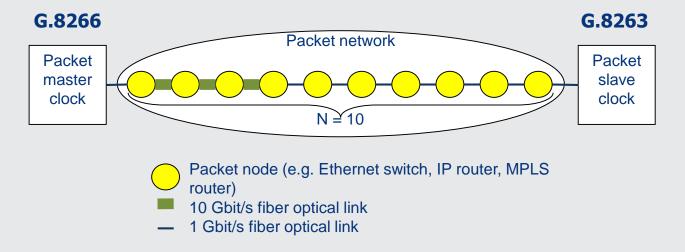


Figure 1/G.8261.1 - HRM-1 for Packet Delay Variation network limits

Note: There is an amendment of G.8261.1 for networks with lower packet delay variation (75µs FPP cluster range instead of 150µs)



G.8263 – Packet-based equipment clocks

- Packet-based equipment clock was defined based on G.8261.1 HRM
- G.8263 includes the following requirements
 - Frequency accuracy
 - Noise generation
 - Packet delay variation noise tolerance
 - Holdover
- Packet delay variation noise tolerance
 - The clock must tolerate the PDV generated by the network
 - For the HRM-1 the clock must meet the output performance specification according to the metrics defined in G.8261.1
 - 1% of the timing packets sent by the packet master remain in the 150 μs fixed cluster range, starting at the floor delay in every observation window of 200 s.





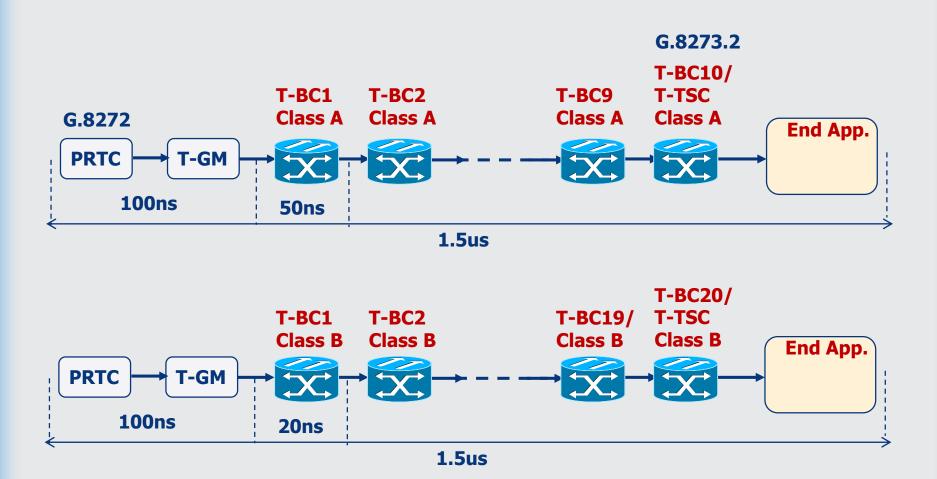
Equipment Clocks

- Clocks for Frequency
 - G.8262 Timing characteristics of Synchronous Ethernet Equipment slave clock (EEC)
 (Consented)
 - G.8263 Timing Characteristics of Packet based Equipment Clocks (PEC) and Packet based Service Clocks (PSC) (Consented)
 - G.8266 Timing characteristics of telecom grandmaster clocks for frequency synchronization
- Clocks for Time/Phase
 - > G.8272 Primary Reference Timing Clock (PRTC) specification
 - G.8273 Clock General Requirements (Consented)
 - > G.8273.1 Telecom Grand Master specification
 - > G.8273.2 Telecom Boundary Clock specification
 - ➤ G.8273.3 Telecom Transparent Clock specification
 - > G.8273.4 Timing characteristics of assisted partial timing support slave clocks





G.8271.1 Architecture



Note: The network limit of 1.5us also accounts for other sources of noise (e.g. holdover, link asymmetries, syncE rearrangements)

PRTC = Primary Reference Time Clocks

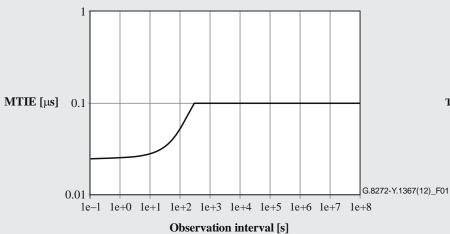
T-GM = Telecom Grand Master



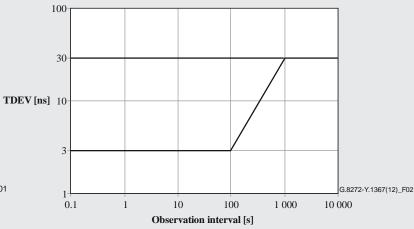


G.8272 Primary Reference Time Clock

- G.8272 includes the following requirements
 - Time error in locked mode
 - Wander in locked mode
 - Jitter
 - Holdover is under study



G.8272/Figure 1 – MTIE as a function of an observation (integration) period t



G.8272/Figure 2 – TDEV as a function of an observation (integration) period t





G.8273.2 Telecom boundary clocks and telecom time slave clocks

- G.8273.2 includes the following requirements
 - Physical layer frequency performance requirements
 - Constant Phase/Time Error and Dynamic Time Error Noise generation
 - Constant phase/time error generation
 - Dynamic time error (dTE) noise generation
 - Noise tolerance
 - Noise transfer
 - Phase/time error due to a rearrangement of the physical layer frequency transport (e.g. SyncE, SDH)
 - Holdover is under study
- Two classes of Telecom Boundary Clock (T-BC) and Telecom Time Slave Clock (T-TSC)

T-BC /T-TSC Constant TE	Maximum Constant Time
Classes	Error (ns)
A	50
В	20

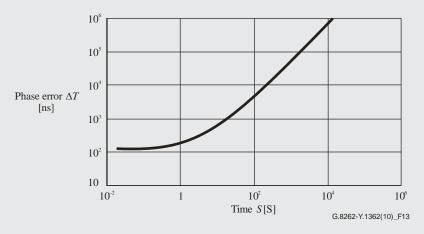
G.8273.2/Table 1 - T-BC Constant Time Error Classes





Physical Layer Assistance

- G.8273.2 uses PTP to transport of time, and physical layer clock (SyncE/SDH) to transport frequency
- The use of physical layer clock is important for Time holdover
 - If an G.8262 EEC-option 1 type of oscillator is used for T-BC, and if the holdover relies only on the oscillator, then the phase will be out of spec in less than a 100 seconds

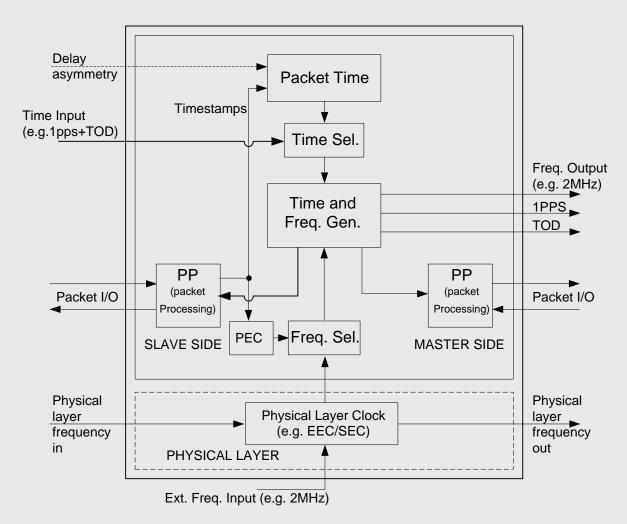


G.8262/Figure 13 – Permissible phase error for an EEC-Option 1 under holdover operation at constant temperature





T-BC Functional Model

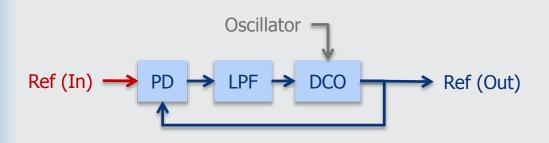


G.8273.2/Figure A. 1: Boundary Clock Model

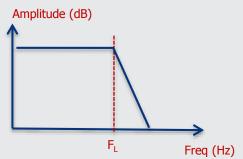




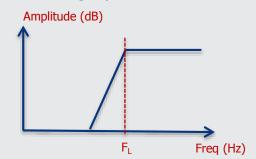
PLL Response to Different Noise Sources

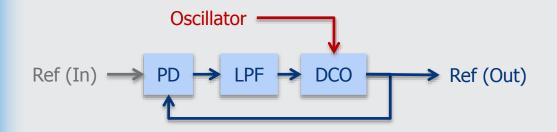


PLL is a low-pass filter for input noise



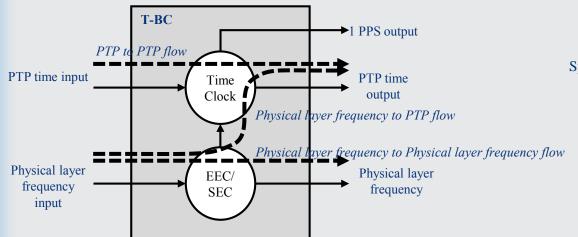
PLL is a high-pass filter for oscillator noise



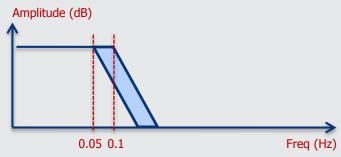




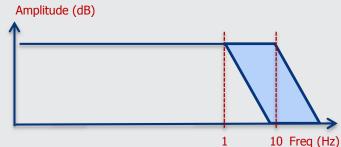
T-BC, T-TSC Transfer Function



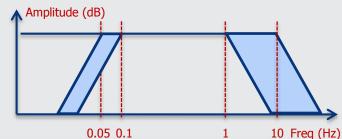
PTP input to PTP/1PPS output: 0.05-0.1 Hz low-pass filter



SyncE input to SyncE output: 1-10 Hz low-pass filter



SyncE input to PTP/1PPS output







Summary

- Standardizing clocks is not trivial, but it is very important
 - Allows interoperability, limits noise accumulation in a chain of clocks
- It is dependent on the Network Architecture
- Several parameters of the clock are dependent on the number of clocks that are in tandem
 - Control of wander and jitter are important
 - Proper PLL design are important (e.g. gain peaking)
- Clocks for Frequency has been standardized
- Clocks for phase/time for full support from the network has been standardized
- ITU is still working on standardizing clocks for phase/time with partial support from the network



