Time-Awareness in the Internet of Things

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Cisco White Paper

White Paper

Embracing the Internet of Everything To Capture Your Share of $14.4 Trillion

More Relevant, Valuable Connections Will Improve Innovation, Productivity, Efficiency & Customer Experience

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Doug Handler

To get the most value from IoE, business leaders should begin transforming their organizations based on key learnings from use cases that make up the majority of IoE's Value at Stake.

Executive Summary

- The Internet of Everything (IoE) creates $14.4 trillion in Value at Stake – the combination of increased revenues and lower costs that is created or will migrate among companies and industries from 2013 to 2022.
- The five main factors that fuel IoE Value at Stake are: 1) asset utilization (reduced costs) of $2.5 trillion; 2) employee productivity (greater labor efficiencies) of $2.5 trillion; 3) supply chain and logistics (eliminating waste) of $2.7 trillion; 4) customer experience (addition of more customers) of $3.7 trillion; and 5) innovation (reducing time to market) of $3.0 trillion.
- Technology trends (including cloud and mobile computing, Big Data, increased

GE White Paper

Figure 2. Rise of the Industrial Internet

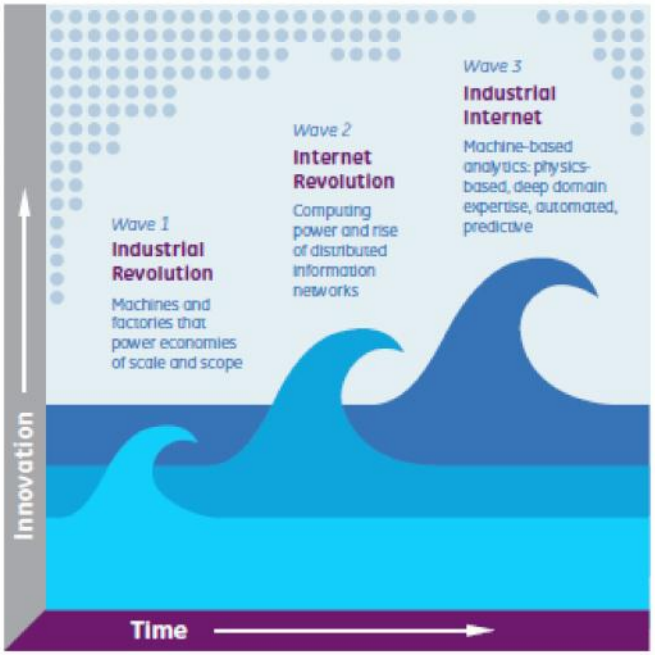
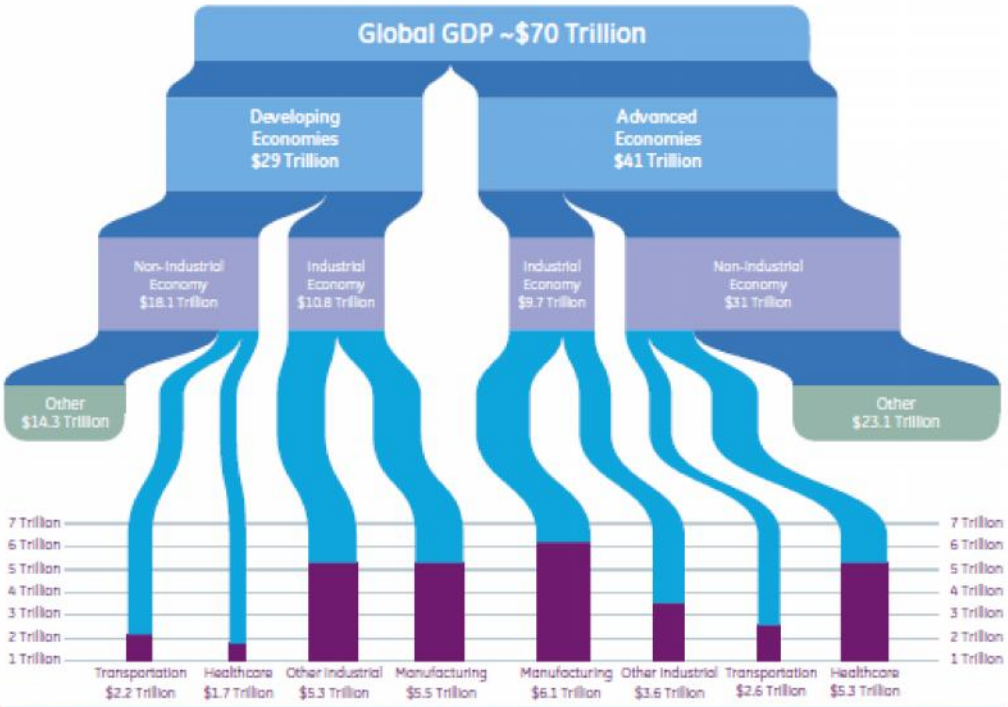


Figure 5. Industrial Internet Potential GDP Share

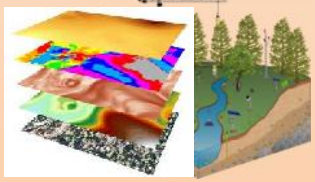


Industrial Internet opportunity ($32.3 Trillion) 46% share of global economy today

Source: World Bank, 2011 and General Electric

A Broad Set of Applications

Predictive maintenance



Enable New Knowledge

Energy Saving (I2E)

Intelligent Buildings

Defense

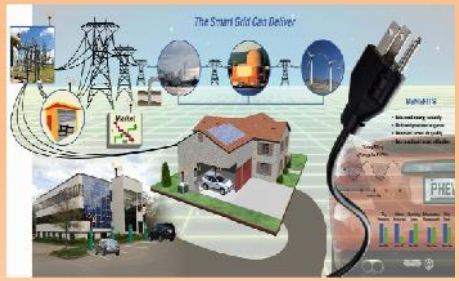
Industrial Automation

Transportation and Connected Vehicles

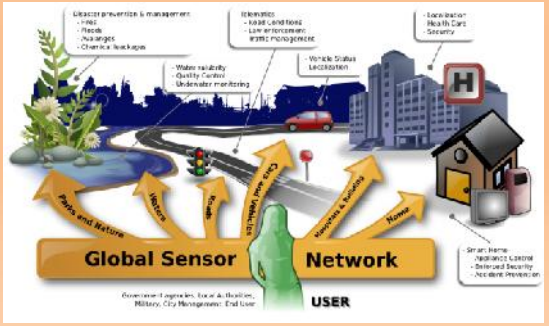
Enhance Safety & Sec

Agriculture

Healthcare



Smart Grid

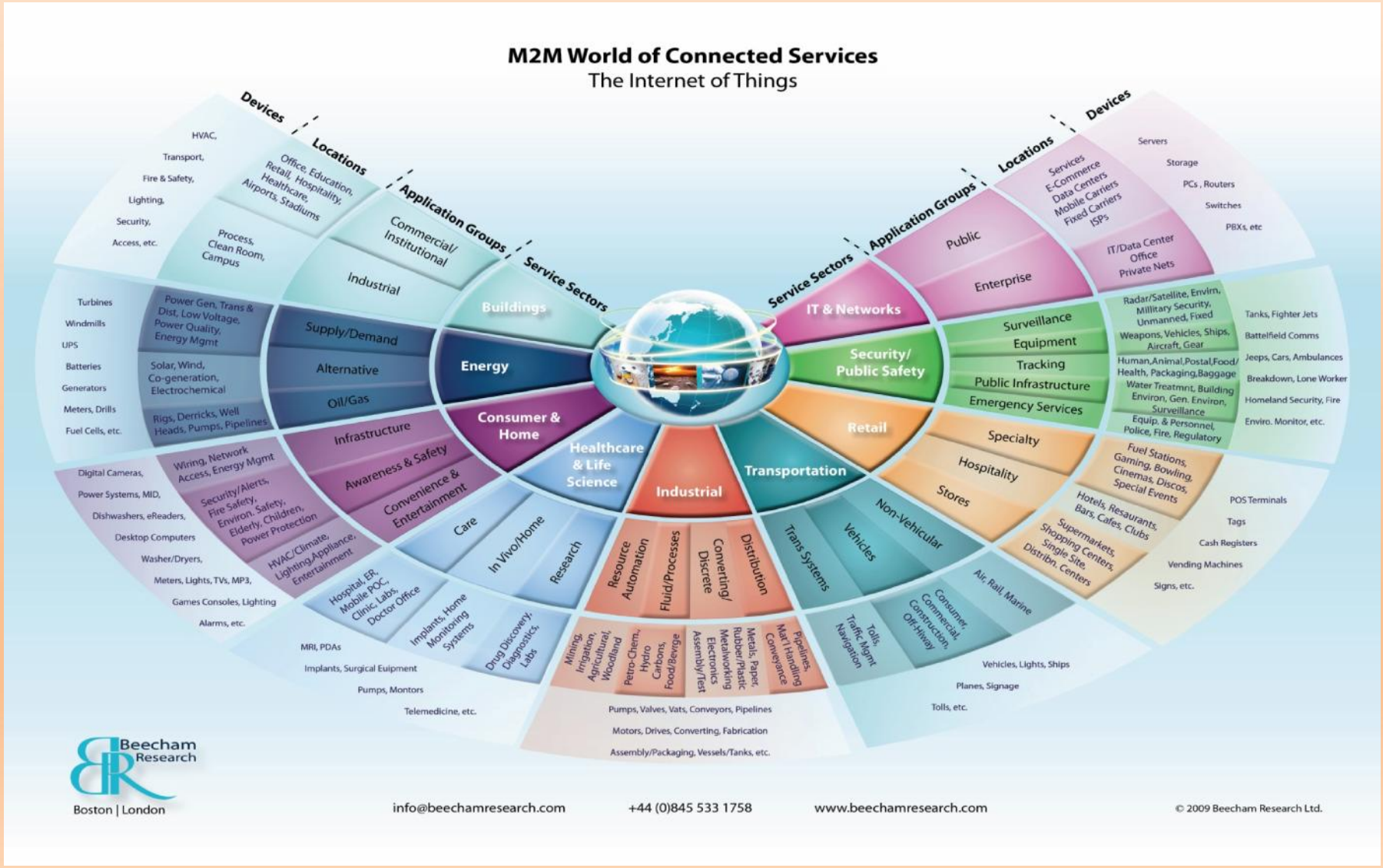


Smart City

Smart Home

Source: Cisco (flavio@cisco.com)

Machine-to-Machine (M2M) Services



We Need a New Network:

A Timing Network is both Physical and Virtual

Timing Network is both Physical and Virtual !

The IoT Will Need Synchronization

- Optimal data techniques obstruct synchronization
  - Computers, software and networks encapsulate functions
  - Sync is a physical signal, and only gets worse as it is detaches from the physical system
  - Current dependence on GPS, problems of availability and vulnerability
- Internet of Things requires New Paradigms for combining Time and Data
  - Need determinism and security in networks
  - Need to be able to design time correctness independent of hardware
  - Timing is currently a only performance metric

TAACCS Initiative

http://taaccs.org/

Critical Research Needs:
New Paradigms

1. **Oscillators** in the network will require a range of performance and cost, as well as ensembling methods, that challenge the state-of-the art
2. **Time Transfer Systems** will need to deliver signals to orders of magnitude more endpoints than currently, with both specified accuracy and integrity, and by traversing both wired and wireless systems
3. **Time Aware Networks** will need development in a number of areas:
    1. **Network equipment** hardware and software will need designs that support and utilize time awareness
    2. Development of time aware and controlled networks requires research in both **propagating and using timing signals**
    3. Time awareness is a critical factor in **controlling latency** in networks, which is crucial to tele-surgery, online gaming, the financial industry and other areas
    4. Timing and analysis for **performance monitoring** is a challenge for maintenance
    5. **Spectrum bandwidth utilization** can be optimized with precision timing

Critical Research Needs:

New Paradigms

4. **Timing support** for applications will need cross-discipline research in the following areas:
    1. Hardware and software support of **predictable execution** will need to balance the depth of change in systems with cost and implementation

Focus in next slides

    2. Timing across **interfaces** will require standards and latency control both between CPU and in crossing network domains
    3. **Scale** issues in supplying time to large numbers of systems

5. **Development environments** will need the ability to specify timing accuracy independent of the hardware that systems are running on
6. **Applications** can make innovative use of time, and will further stimulate the development of these other items.

Time-Aware Computer HW and SW

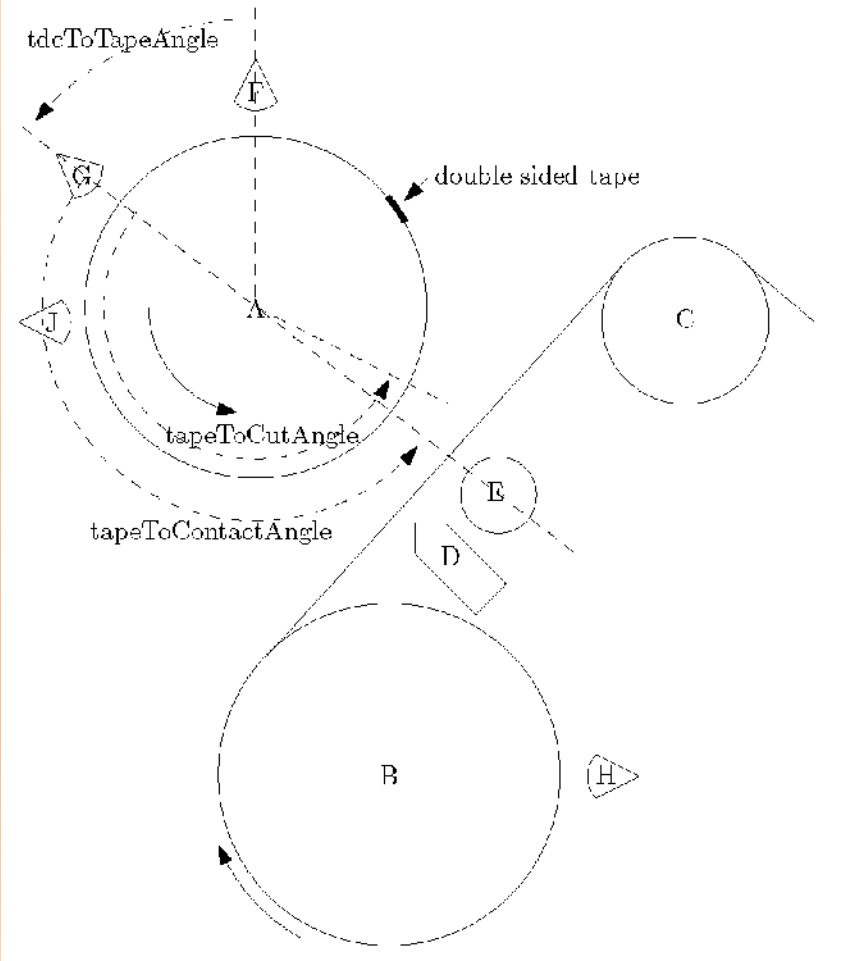
- "The ultimate goal is to enable CPS system timing that is *correct by construction*"
- What does this mean:
  - A timing abstraction constructed to be correct
    - Analyze timing requirements
    - Create an abstract model – no specific HW – but with precisely specified timing
  - Implementation of the abstraction
    - Design environment compiles into processor or indicates it's not possible
    - Programming languages have time semantics, which along with HW are time aware. Timing behavior can be precisely specified (with minimal and known uncertainty) by software or FPGA developer
  - Upgrades of HW or SW do NOT require a redesign!

Real-Time Systems Today

- Determinism requires special HW
  - Cannot be achieved in SW – SW at best is modelled statistically for maximum latency
  - Specially designed FPGAs, etc. enforce precision timing
  - The entire system may need calibration for timing accuracy
- Any change in HW or SW can trigger a major re-calibration
- Programming languages do not allow timing accuracy

An example of a system with critical timing requirements- The “Flying Paster”

(next 2 slides from “Using Ptides and Synchronized Clocks to Design Distributed Systems with Deterministic System-wide Timing”,Derler.et.al., ISPCS 2013-Lemgo)



1. When feed roll B is nearly empty
2. Reserve roll A is brought to matching surface velocity
3. The position of the tape is observed and angles are calculated
4. When B is at a critical radius and the tape is at the “contact” angle, E forces the two feeds together
5. A short time later D cuts the B feed leaving A as the primary feed

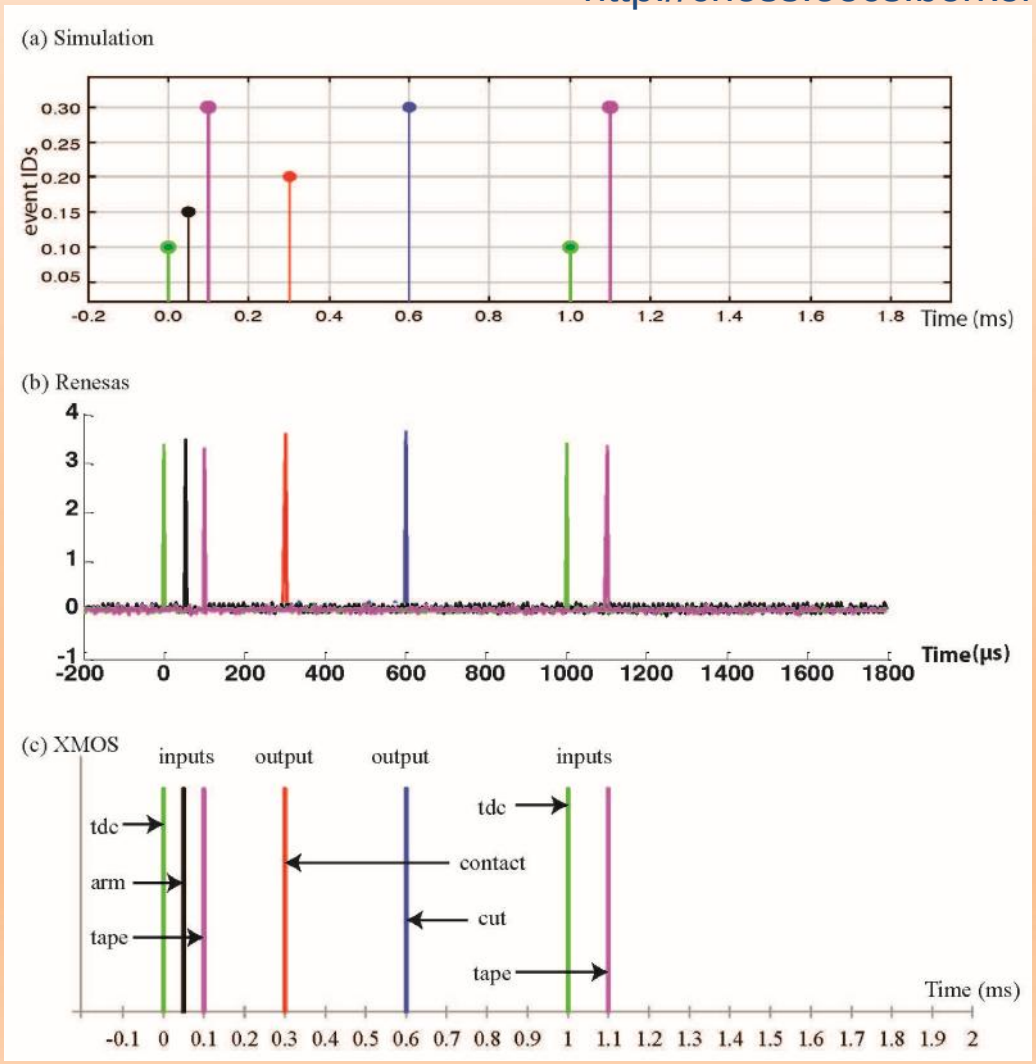
http://www.youtube.com/watch?v=wYRGiXMUzA4

This slide due to John Eidson

Embedded systems- especially distributed systems.

Designers should be able to design, simulate, and code generate for multiple targets with guaranteed timing!

http://chess.eecs.berkeley.edu/ptides/



This slide due to John Eidson

Comments on the Flying Paster example

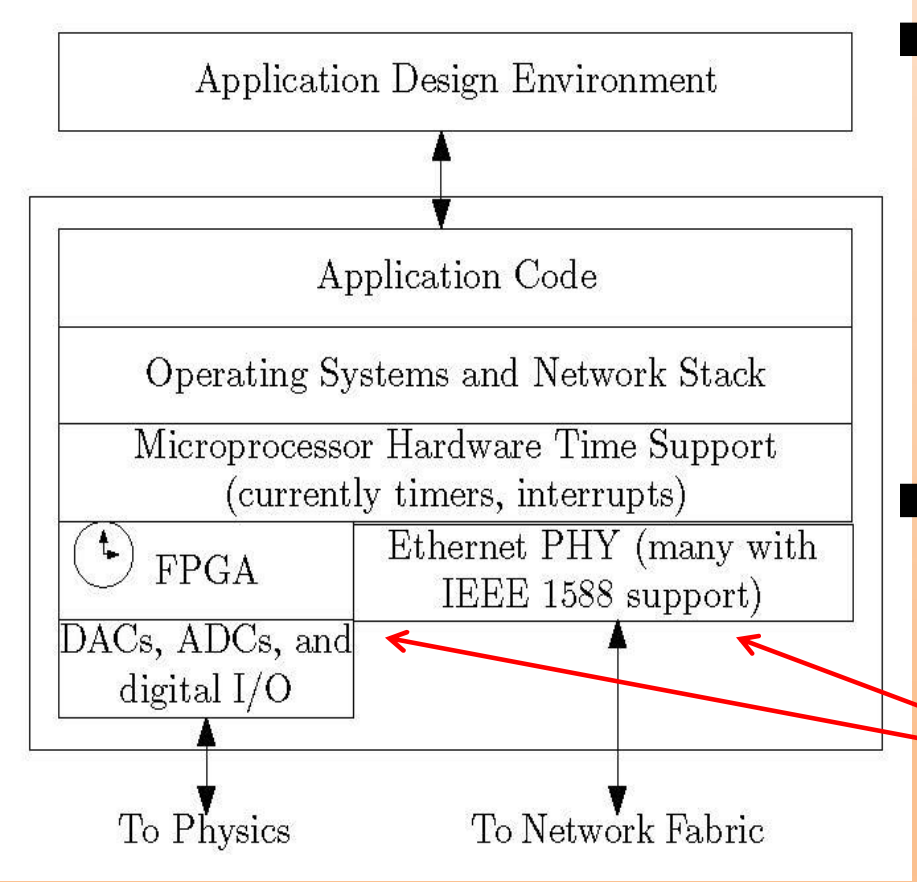
The Ptides implementation shown demonstrates:

- Physical time vs. Model time with correspondence enforced only at key points, e.g. sensors and actuators
- Same design compiled to two different platforms => identical timing to within clock resolution (8ns)

The "You Tube" video no doubt used a time-triggered architecture where a strict: sense, compute, actuate cycle is enforced with hardware supported sense and actuation timing

This slide due to John Eidson

Cyber Physical Systems Node and Environment, Currently

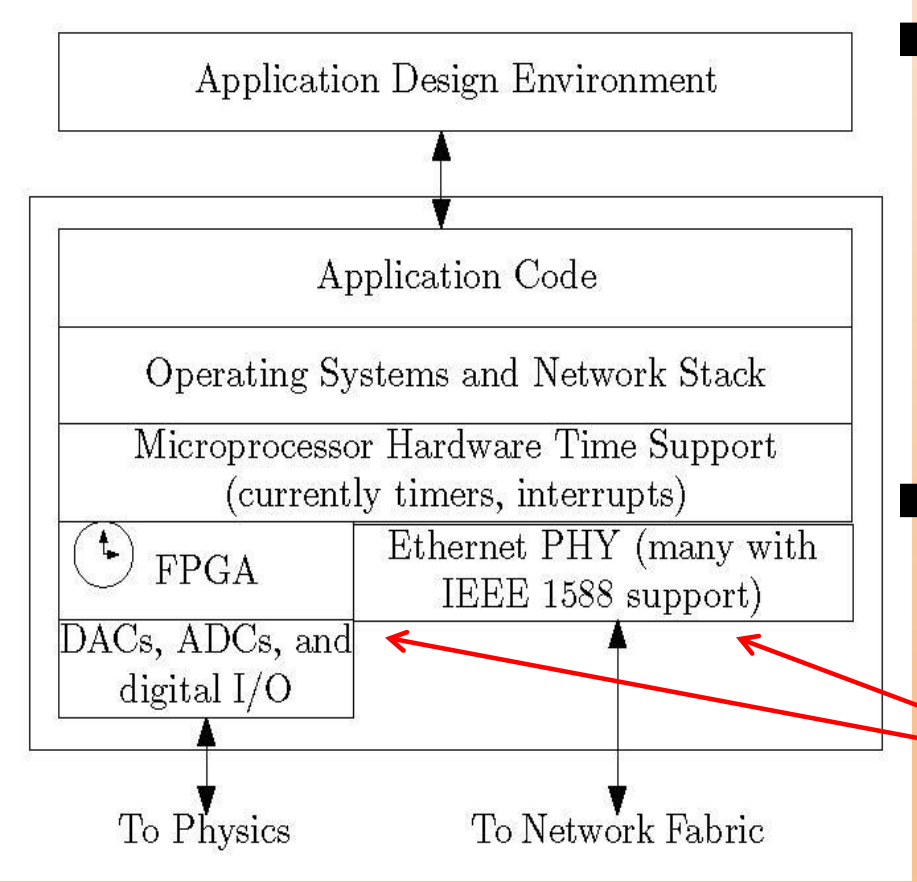


- No semantics of accurate time neither in design, nor languages
- Possibly bounded TIs
- Almost never stable (deterministic)
- Hence robust, correct by construction solutions cannot be done here!

- Precise TIs
- Can be accurate (traceable to SI second or TAI)
- Hence robust, correct by construction is possible (but not very flexible)

This slide based ones by John Eidson

Cyber Physical Systems Node and Environment with Correct by Construction



- Time can be specified as abstraction in model
- Code is Bounded and Time explicit
- I/O is Time sensitive, explicit, and precise
- CPU clock is precise and if needed accurate
- Hence robust, correct by construction solutions can be done here!

- Precise TIs
- Can be accurate (traceable to SI second or TAI)
- Hence robust, correct by construction is possible (but not very flexible)

This slide based ones by John Eidson

Thank you for your attention!

Questions?