

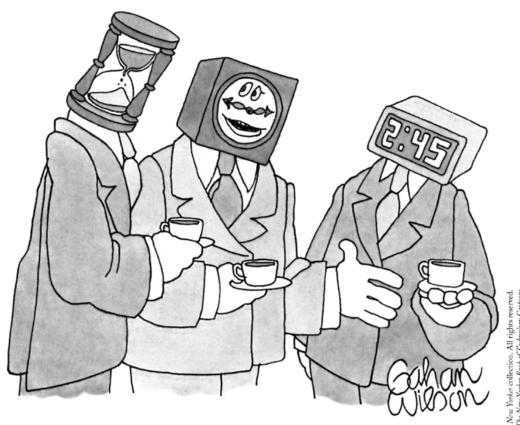
Simple Descriptions, Complex Metrics

A graphical approach to understanding packet clock metrics

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ITSF 2013 – Lisbon, Portugal



"Basically, we're all trying to say the same thing."

- Introduction
- New Metrics
- Lucky Packets
- Floor Population
 - Definitions
 - Limits
 - Example Measurement
- MAFE
 - Definition
 - Example Measurement
- Conclusion

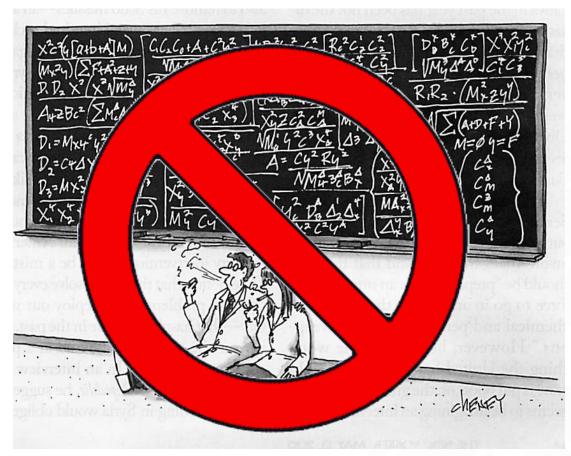
Introduction



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Introduction



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New Metrics



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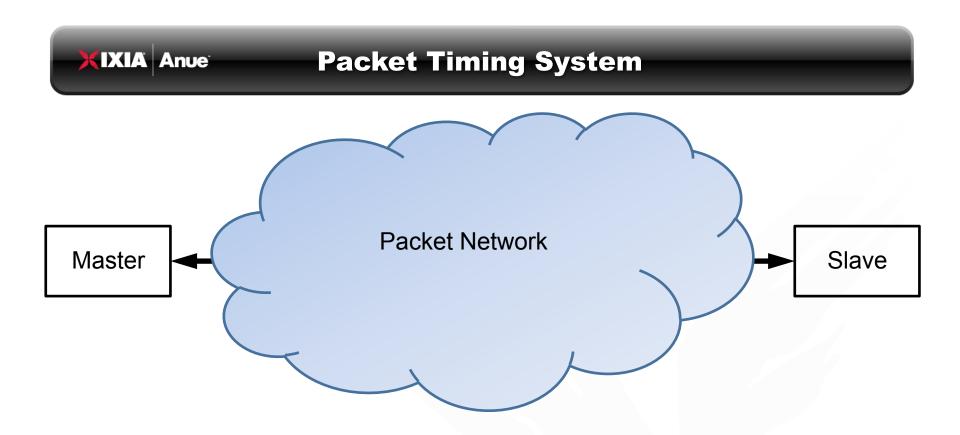
New Metrics

- What are the new metrics?
 - FP<u>C</u>, FP<u>P</u>, FP<u>R</u> (<u>F</u>loor <u>P</u>acket <u>C</u>ount, etc.)
 - MAFE (<u>M</u>ax. <u>A</u>bs. <u>F</u>req. <u>E</u>rr.)
- Where are they used? New ITU Rec's
 - FPP & MAFE: Defined in G.8260
 - FPP: Network limit in G.8261.1 (1%)
 - FPP: Slave tolerance limit in G.8263 (1%)



What do they measure?

- Floor packet metrics measure:
 - How many packets go fast
 - Plotted versus time
 - It will tell you <u>when</u> a problem happened
- MAFE measures:
 - Peak frequency error implied by lucky packets
 - Helps estimate packet slave performance
 - Plotted versus observation interval (τ)



The Floor Population Metrics & MAFE are ways to characterize Packet Delay Variation (PDV) in this system

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XIXIA Anue Quiz: Which of these shows Lucky Packets?







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Lucky Packets

- Packets that experience near minimum delay are Lucky
 - They spend little or no time waiting in queues
 - They are fortunate to avoid congestion in the network
- KEY: PDV of lucky packets is relatively low

Imagine driving home with all the traffic lights <u>GREEN!</u>



Packet Selection

- Two ways:
 - Cluster range (e.g. within 150us of minimum)
 - Percentile range (e.g. 5% of fastest packets)
- Floor population metrics use cluster range
- We'll see MAFE with percentile range

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Cluster Selection Analogy





Cluster Selection Analogy



- Game lasted 1 minute
- Three darts thrown
- Two hit Bull's Eye
- 1 point for Bull's Eye

STATS

- Score=2
- Percent=67% (2/3)
- Rate=2/minute

XIXIA Anue Metric Definitions via Dart Board Analogy

- Floor Packet Count (FPC)
 - The number of times a dart landed in the Bull's Eye
- Floor Packet Percentage (FPP)
 - The percentage of times a dart landed in the Bull's Eye
- Floor Packet Rate (FPR)
 - The rate that darts land in the Bull's Eye (e.g. per minute or hour)
- To apply to packet timing systems:
 - Replace "dart" with "timing packets"
 - Replace "land" with "have delay" (or "are delivered")
 - Replace "Bull's Eye" with "Floor Window"
 - (size of Bull's Eye is analogous to the "cluster range"



The Floor Window (a.k.a. the Bull's Eye)

Window has width, height and vertical position

Width is defined as 200 seconds
 Height is defined as 150 microseconds
 Position of window is based on minimum observed delay
 (NOTE: Not drawn to scale)

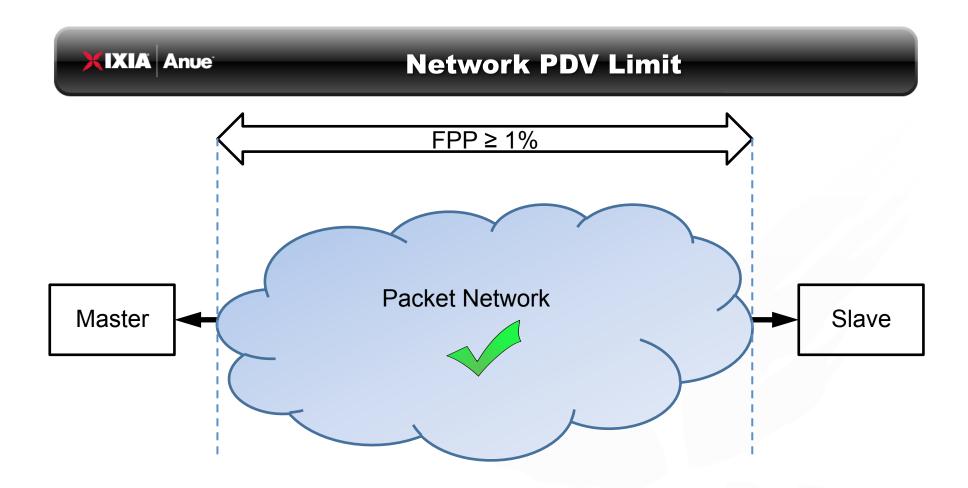
Network PDV Limit (G.8261.1)

The Packet Delay Variation network limit at the point C of figure 3/G.8261.1 for the HRM-1 shown in figure 1/G.8261.1 is defined as follows:

With window interval W = 200s and fixed cluster range $\delta = 150 \mu s$ starting at the floor delay, the network transfer characteristic quantifying the proportion of delivered packets that meet the delay criterion should satisfy

FPP
$$(n, W, \delta) \ge 1\%$$

That is, the floor packet percentage must exceed 1%.



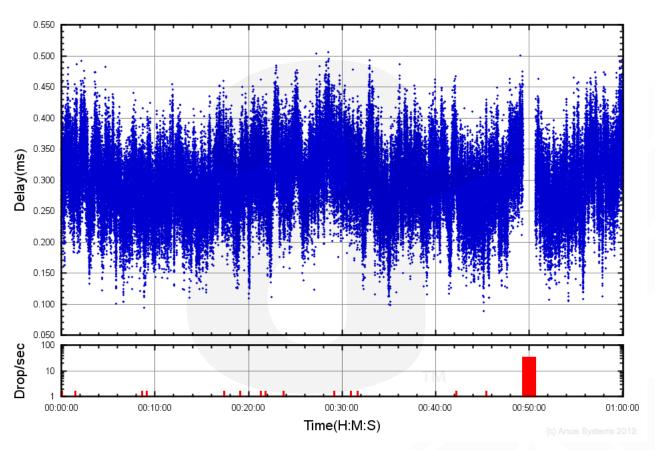
NOTE: This is a relative measurement and doesn't depend on timing packet rate

Example Measurement

- Packet timing system operating at 32 packets per second
- Packet Delay Variation (PDV) based on flicker noise
- Low level of random packet loss (0.01%)
- Brief network outage (80 seconds)
- Steps for calculating FPC, FPP & FPR
 - Find minimum delay
 - Draw FPC graph, explain axes
 - Calculate with sliding window

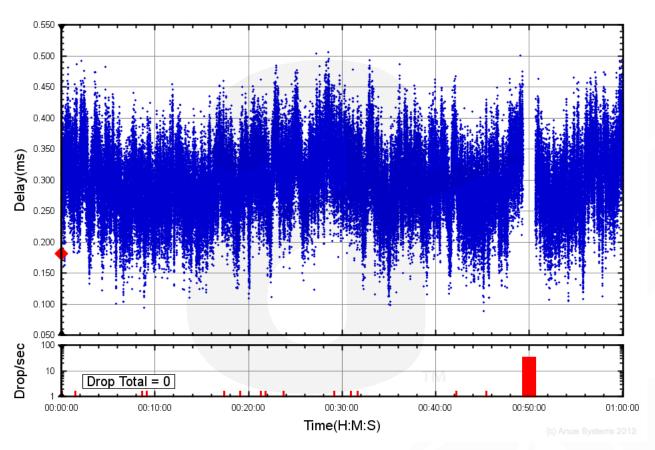


Example PDV with 0.01% Loss (@32 pkt/sec)



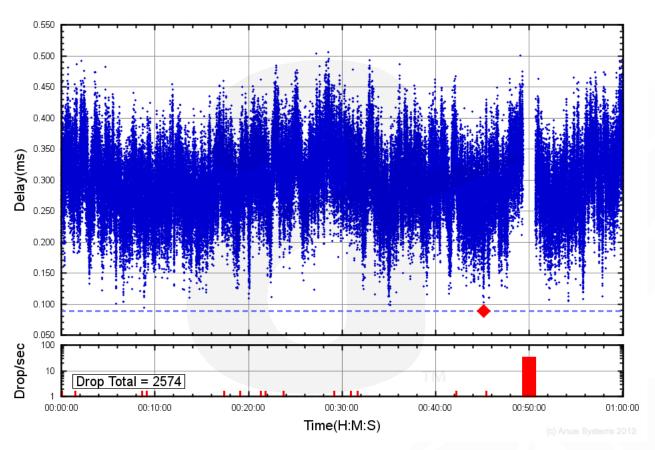


Search for minimum delay value



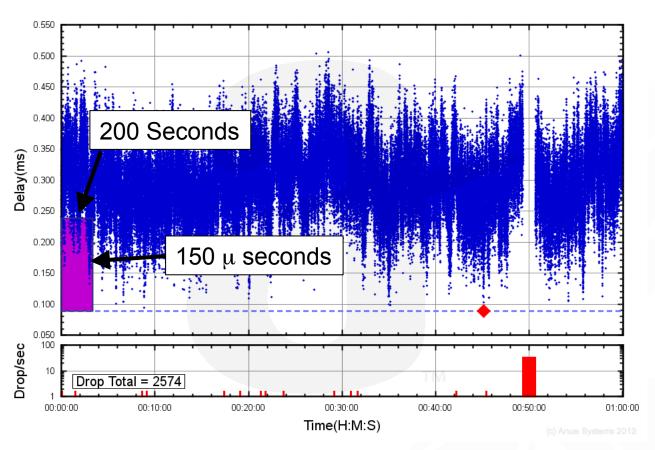


Draw horizontal line for minimum delay



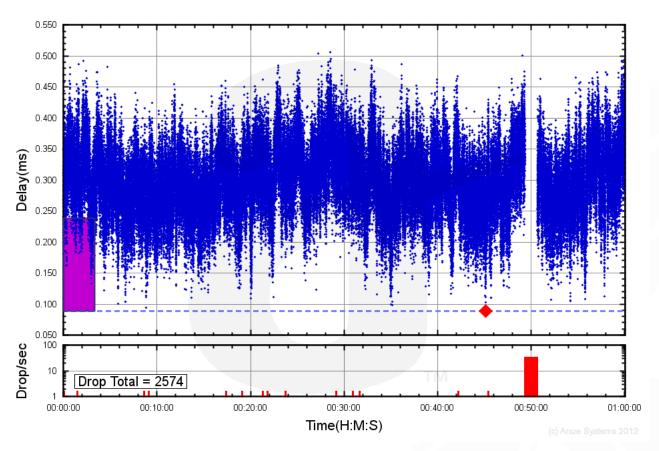


Draw the Floor Window



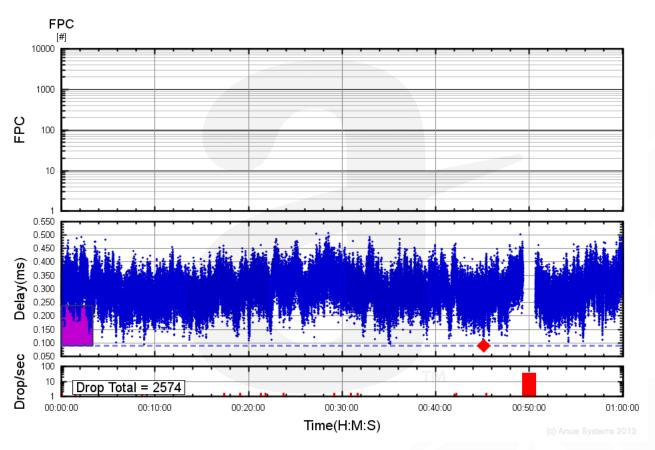


Add the FPC graph



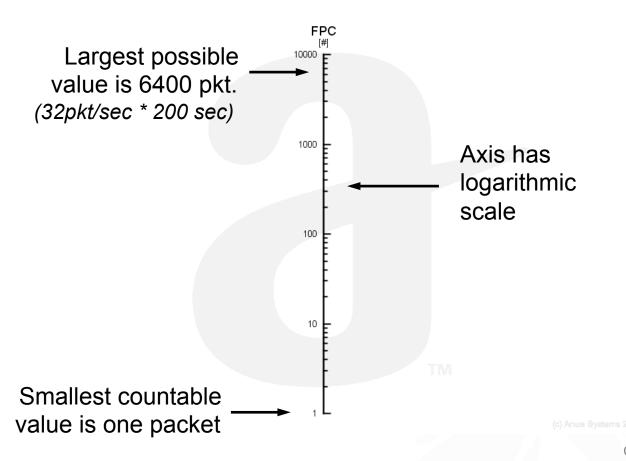


Look at just the FPC Axis



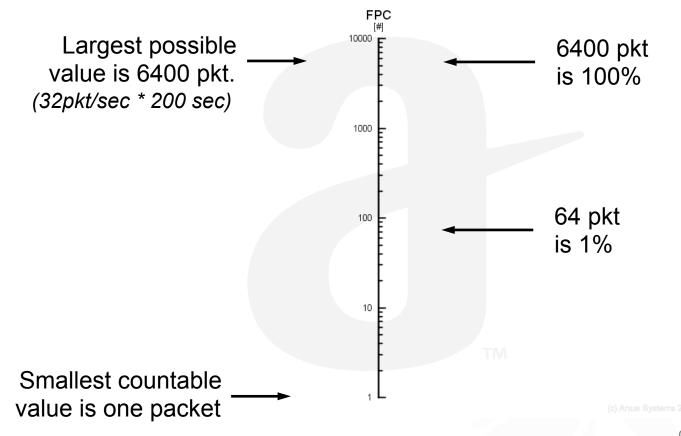


Look at just the FPC Axis



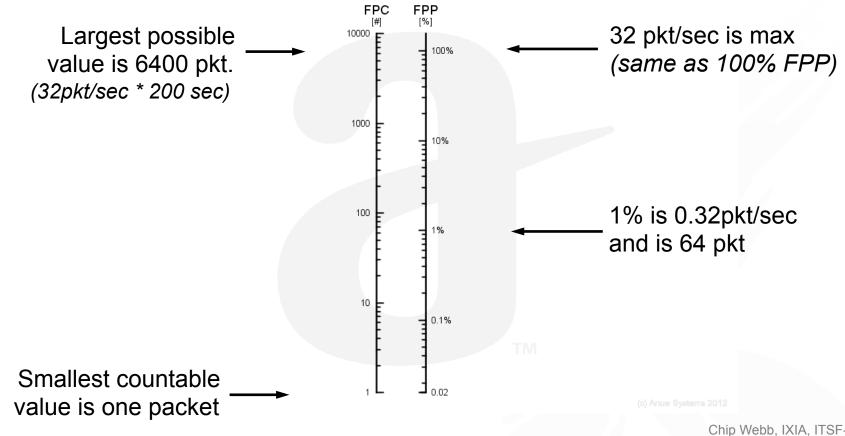


Compare FPC to FPP



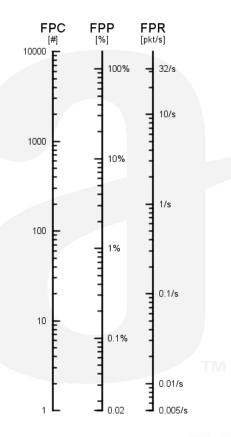


Compare FPC and FPP to FPR





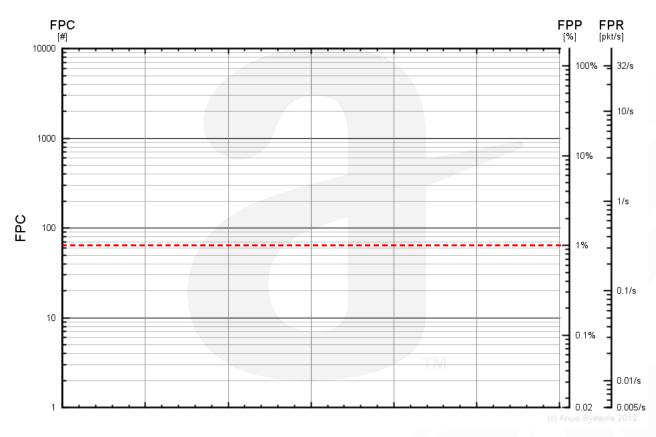
Draw the 1% FPP Limit Line



(c) Anue Systems 2012

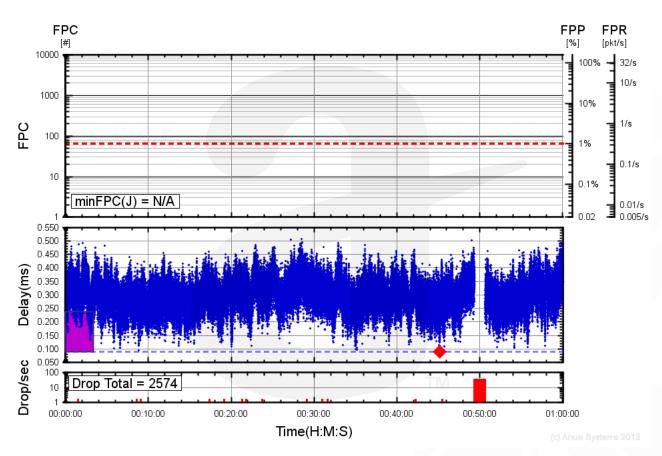


Draw the 1% FPP Limit Line



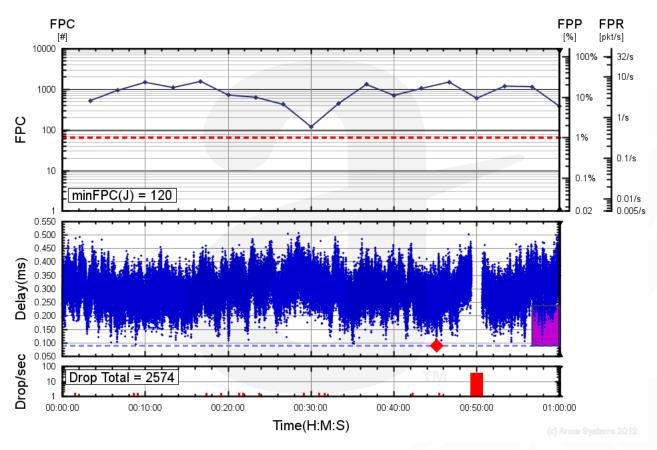


Calculate with Jumping Window



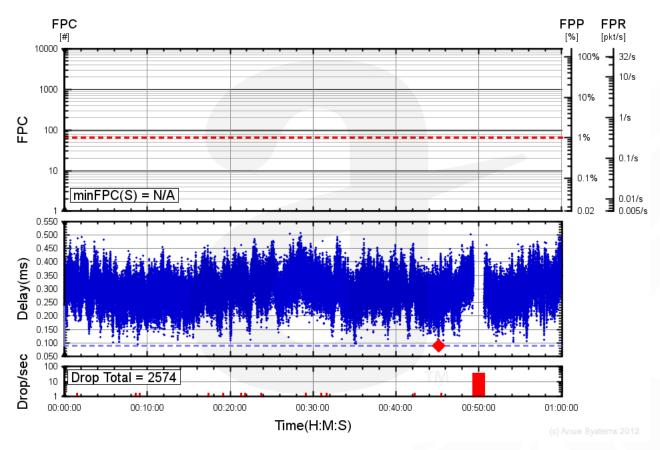


Calculate with Jumping Window



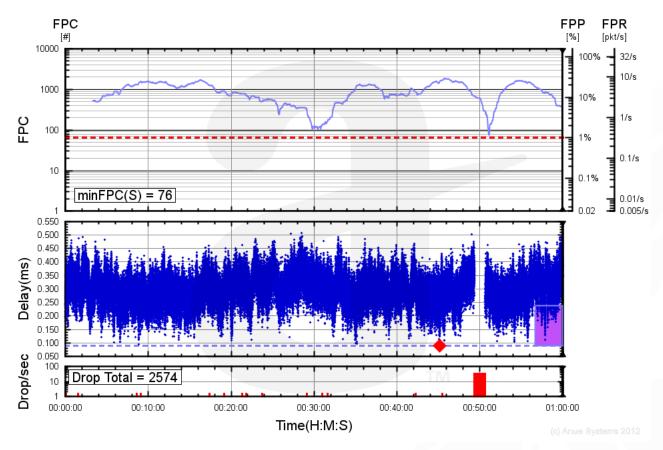


Calculate with Sliding Window



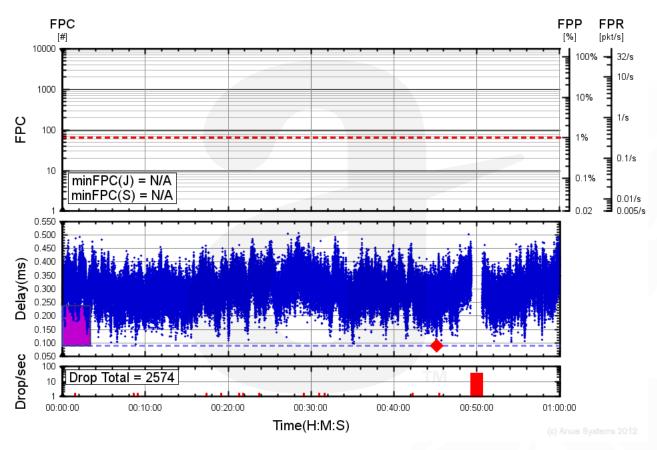


Calculate with Sliding Window





Compare: Jumping/Sliding



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MAFE

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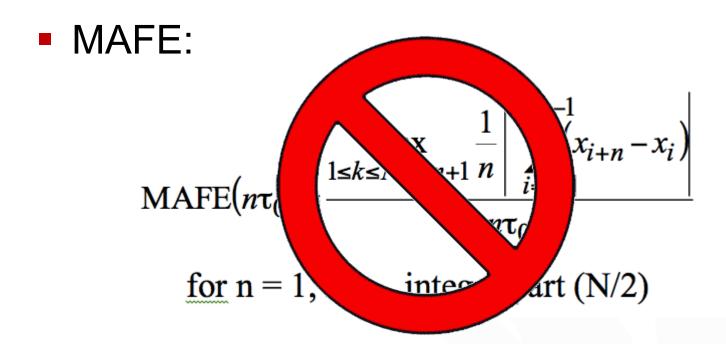


MAFE (in words)

- MAFE measures:
 - Peak frequency error implied by lucky packets
 - Helps estimate packet slave performance
- Helps answer questions like:
 - With a 1 hour averaging period, what is the worst-case frequency offset that will be seen?
- Closely related to MATIE
 - Max. Abs. Time Interval Error



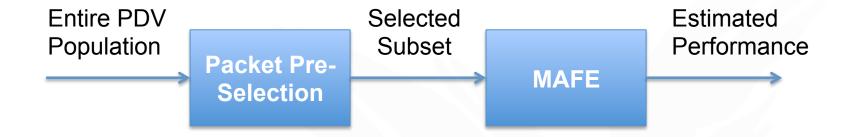
MAFE (in equations)



(Note: this is the MAFE estimator formula from G.8260, eq. I-21)

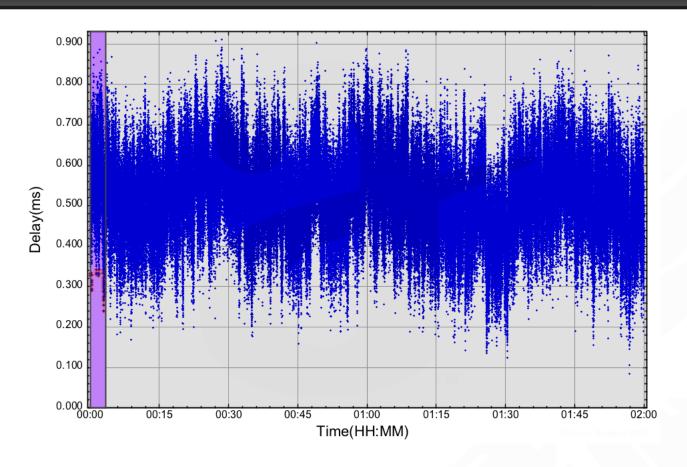


MAFE Overview



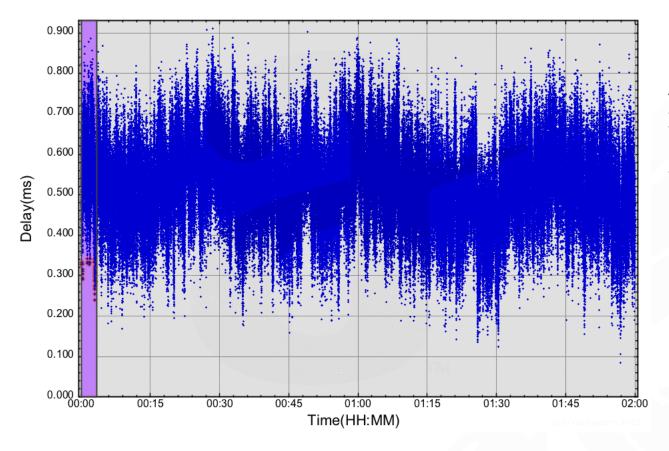


Example PDV for MAFE





Packet Pre-Selection (pick fastest 1%)

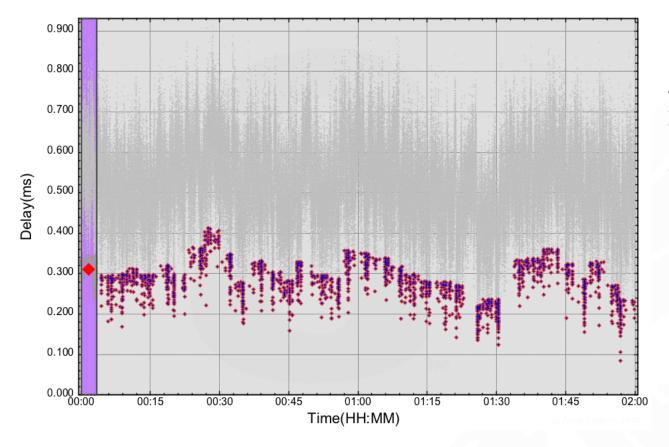


Pre-Selection:

Average of fastest 1% over 200s win. with "jumping"



Packet Pre-Selection (take the average of the 1%)

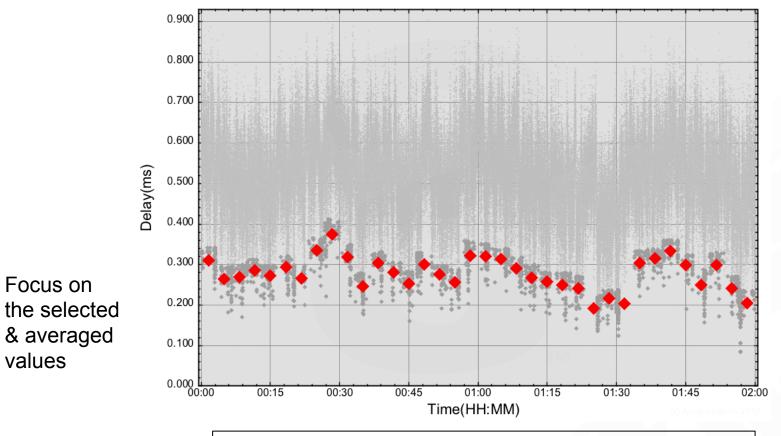


Pre-Selection:

Average of fastest 1% over 200s win. with "jumping"



Packet Pre-Selection Result



Pre-Selection:

Average of fastest 1% over 200s win. with "jumping"

Note: This pre-selection method reduces the number of samples by a factor of 6400

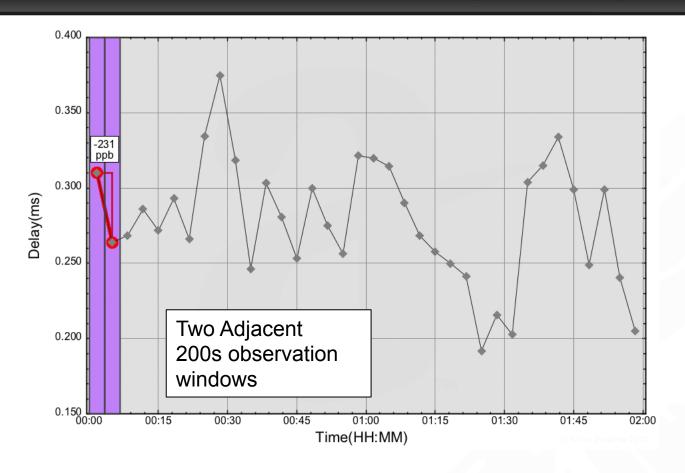
values

Focus on

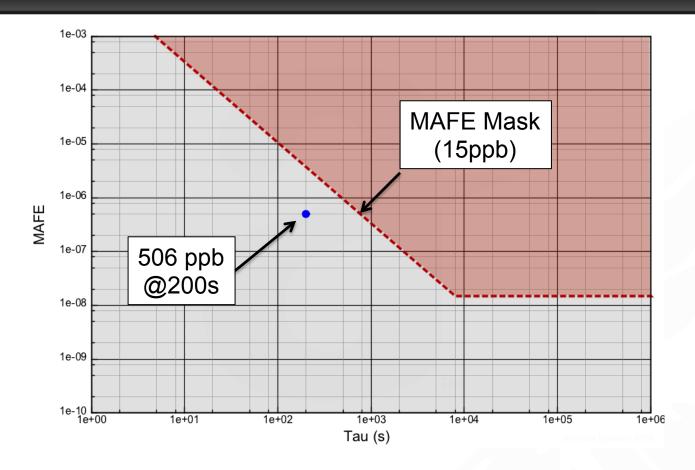
& averaged



MAFE Computation (Tau=200s)

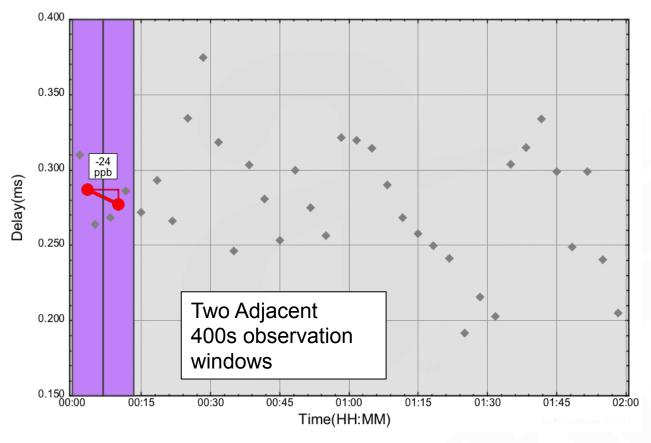


MAFE Plot



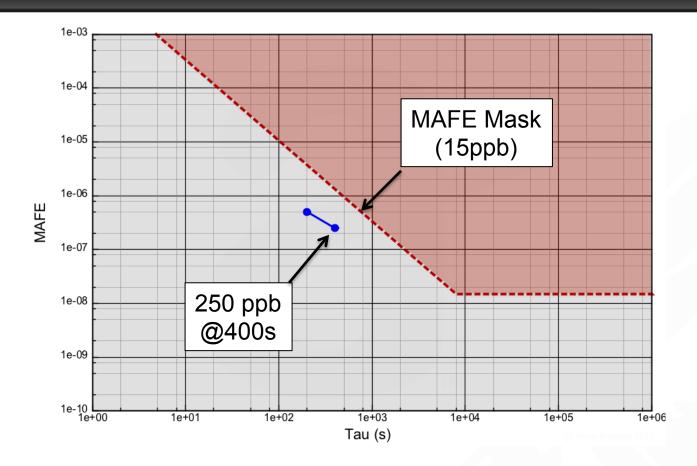


MAFE Computation (Tau=400s)



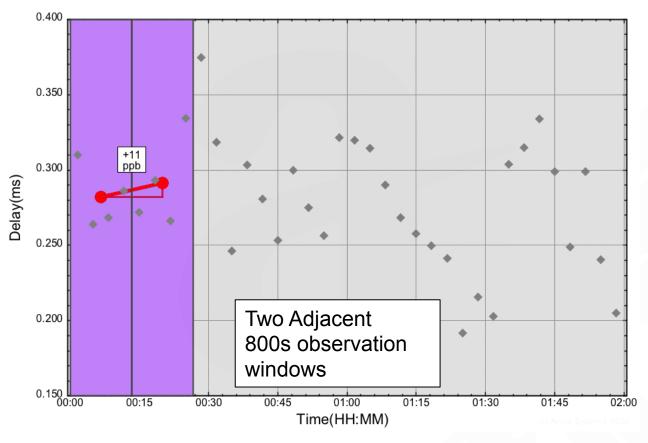
Note: Average the two consecutive selected samples in each window

MAFE Plot



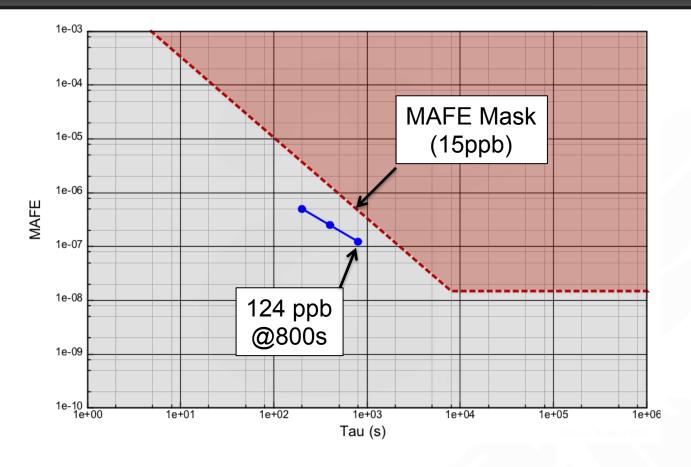


MAFE Computation (Tau=800s)



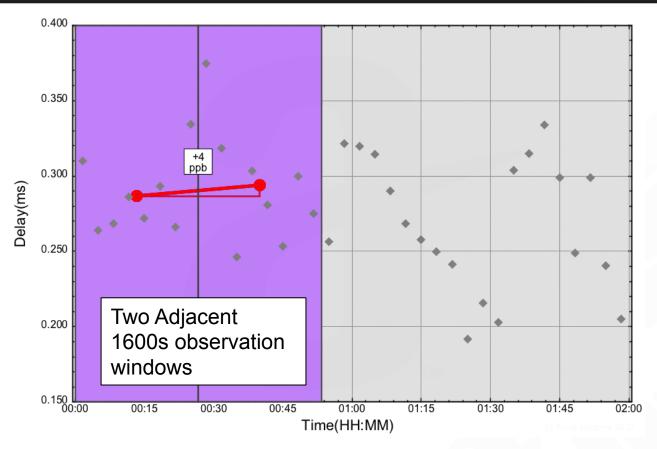
Note: Average the four consecutive selected samples in each window

MAFE Plot



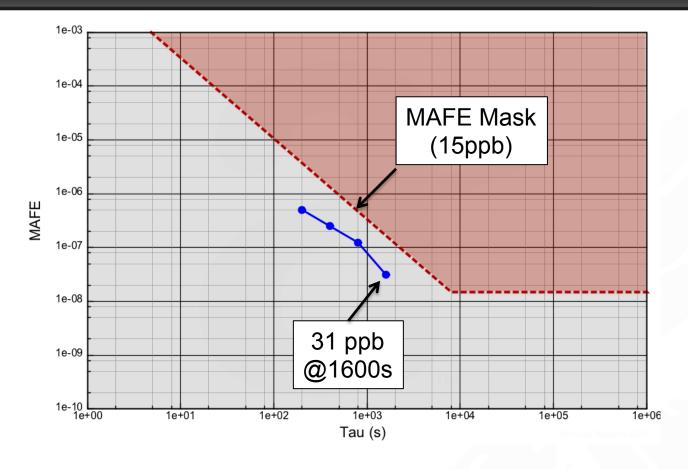


MAFE Computation (Tau=1600s)



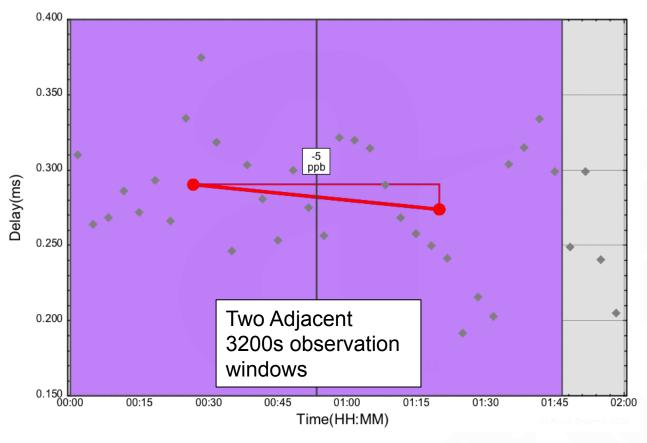
Note: Average the eight consecutive selected samples in each window

MAFE Plot

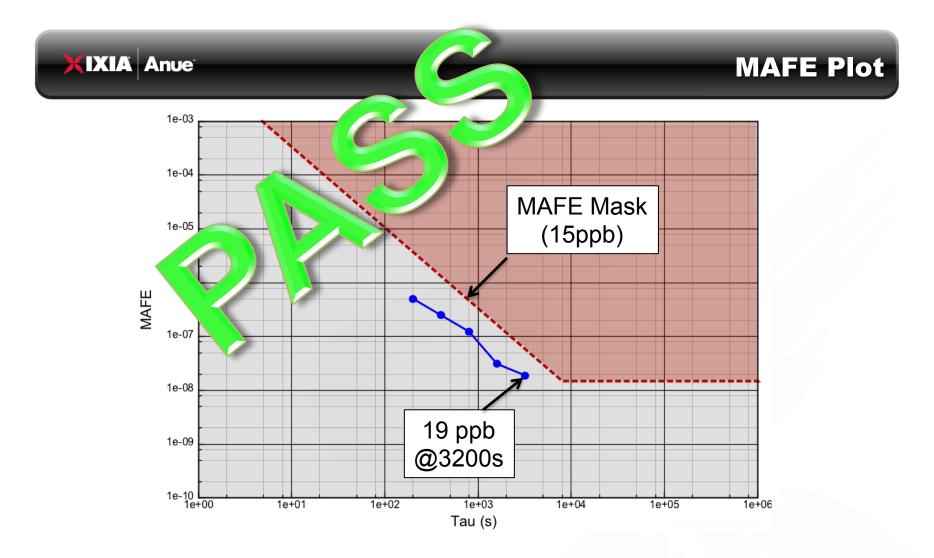




MAFE Computation (Tau=3200s)



Note: Average the sixteen consecutive selected samples in each window



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Floor Population Metrics: In a nutshell



MAFE: In a nutshell



XIXIA Anue Thank You! Questions?





About the Presenter



About Ixia

<u>Ixia</u> provides the industry's most comprehensive converged IP network validation and <u>network visibility</u> solutions.

Equipment manufacturers, service providers, enterprises, and government agencies use lxia's solutions to design, verify, and monitor a broad range of wired, Wi-Fi, and 3G/LTE equipment and networks. Ixia's test solutions emulate realistic media-rich traffic and network conditions so that customers can optimize and validate the design, performance, and security of their pre-deployment networks. Ixia's intelligent network visibility platforms provide clarity into physical and virtual production networks for improved performance, security, resiliency, and application delivery of cloud, data center, and service provider networks.

For more information, visit <u>www.ixiacom.com</u>.



About Chip

Chip is VP, Technology at Ixia, after its acquisition of Anue Systems, where he was cofounder and CTO. He has 20+ years of experience in the design of high-speed networking products. Prior to founding Anue Systems, Chip was a Distinguished Member of Technical Staff at Bell Laboratories. Chip received a Master's degree in Electrical Engineering from Columbia University, and a Bachelor's degree, with honors, from RPI. He has been awarded 14+ patents.