Real-World Testing of On-Path Support

Kishan Shenoi, Chip Webb, Josh Karnes

Ixia

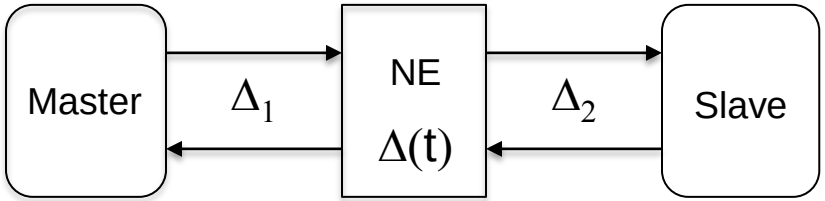
Outline

- On-path Support – timing perspective
  - Principles
  - Types of on-path support (BC and TC)
- Testing Configurations
- Experience with boundary clock and transparent clock testing
- Concluding Remarks

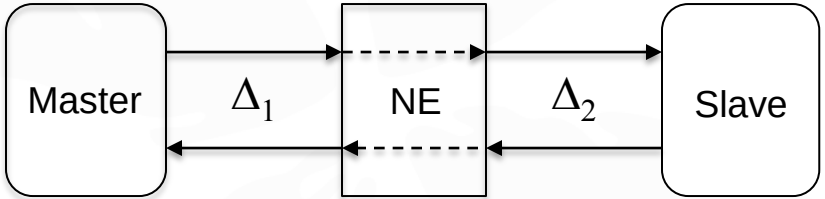
Principles of on-path support

- Time transfer accuracy bounded from below by transit delay asymmetry (Δ_1 and Δ_2)
- Frequency transfer accuracy impaired by transit delay variation
- On-path support attempts to:
  - Minimize (eliminate) transit delay asymmetry in NE
  - Minimize (eliminate) transit delay variation in NE
  - Time transfer error is minimized [≥ (Δ_1 + Δ_2)]

PTP-unaware Network Element



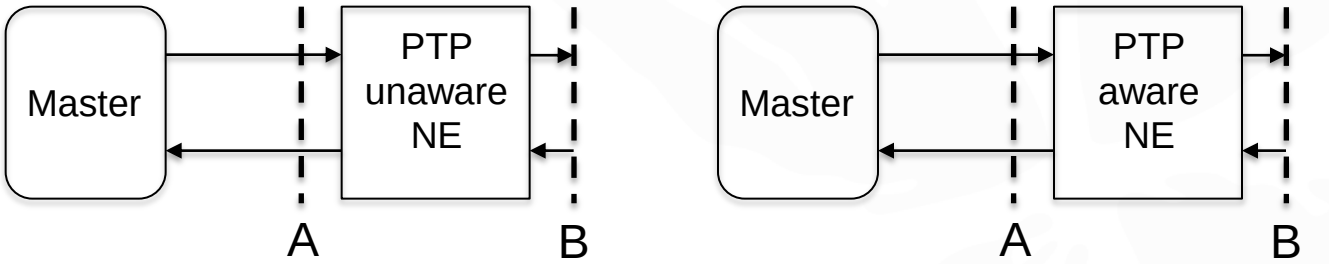
PTP-aware Network Element



$\Delta(t) \approx 0$

Principles of on-path support

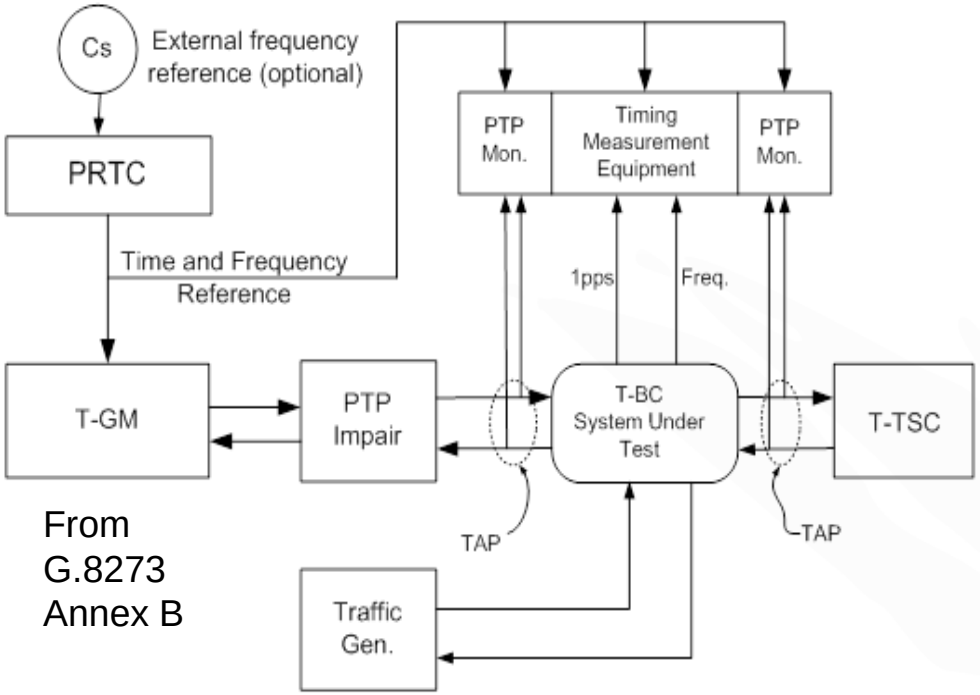
- Consider (hypothetical) slave deployed just before or just after NE
  - *Without* on-path support the slave at B has *different* time/wander behavior compared to the slave at A; performance is load dependent
  - *With* on-path support the slave at B has (ideally) the *same* time/wander behavior compared to the slave at A; performance *should be load independent*
- Two forms of on-path support:
  - Boundary clock — "regenerates" master
  - Transparent clock — acts "invisible" (by providing correction)



Testing Boundary Clocks

- Boundary Clocks
  - Provide PTP services at network junctions with, possibly, multiple master ports to supply downstream clocks from one slave port
  - Comparatively new devices and industry is still learning
  - Boundary clocks must fit into existing network topologies
- Testing Challenges
  - Boundary Clocks may introduce non-linear timing errors whose effects are analogous to time error produced by busy switches
  - Boundary Clocks may have 1pps outputs to test the “slave” side of BC but that does not address the master port
- Methods for accurately identifying and analyzing the timing impairments introduced by a boundary clock are maturing

Testing on-path support



From G.8273 Annex B

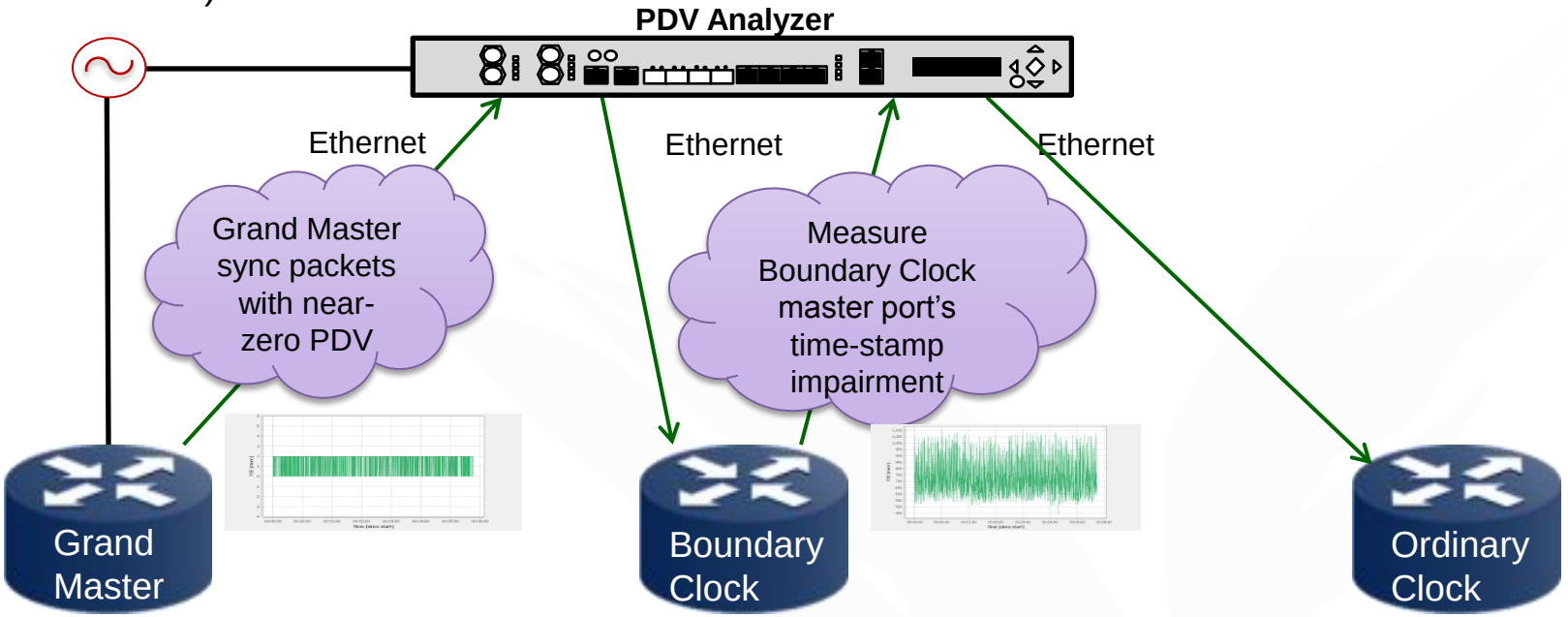
- Arrangement for testing on-path support described in G.8273 Annex B
- Notes:
  - PTP Impair – models time error introduction, if any, between GM and BC/TC
  - Traffic Gen. – represents traffic inserted to investigate behavior of BC/TC in different load conditions
  - BC may provide a frequency as well as 1pps output
  - PTP Mon. function emulates a slave time/frequency recovery but uses packets generated by the other devices

BCs and TCs– Not Ordinary Switches

- In most conventional methods boundary clocks and transparent clocks are tested as a neighbor to a slave clock and the test result derived from the slave's output
  - G.8273 considers direct evaluation of on-path support
- Real-world testing reveals surprising results
  - Boundary and transparent clocks do introduce impairments
    - There is a source of time error impairment (static and dynamic) caused by a boundary/transparent clock that must be evaluated
    - Impact of a boundary clock on frequency recovery may be comparable to that of an ordinary switch with no on-path support (TC under study)
- Methods of testing that consider **both** static and dynamic impairments are required for validating time/phase transfer

Boundary Clock Test Scenario #1
Evaluate Boundary Clock Impairment

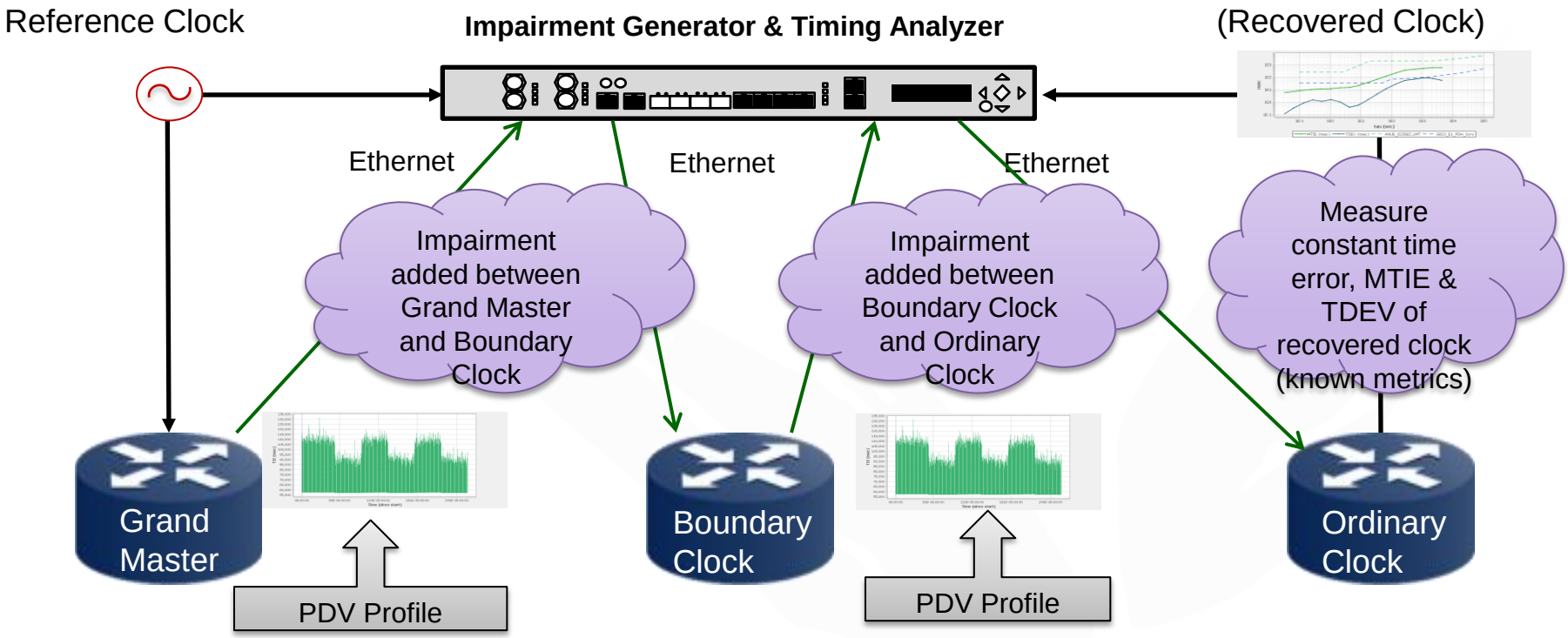
(Reference Clock)



Time-stamp impairment created by the Boundary Clock (Master) looks like time error (static and dynamic) to downstream slave

Boundary Clock Test Scenario #2

Impact of Boundary Clock with emulated impairment



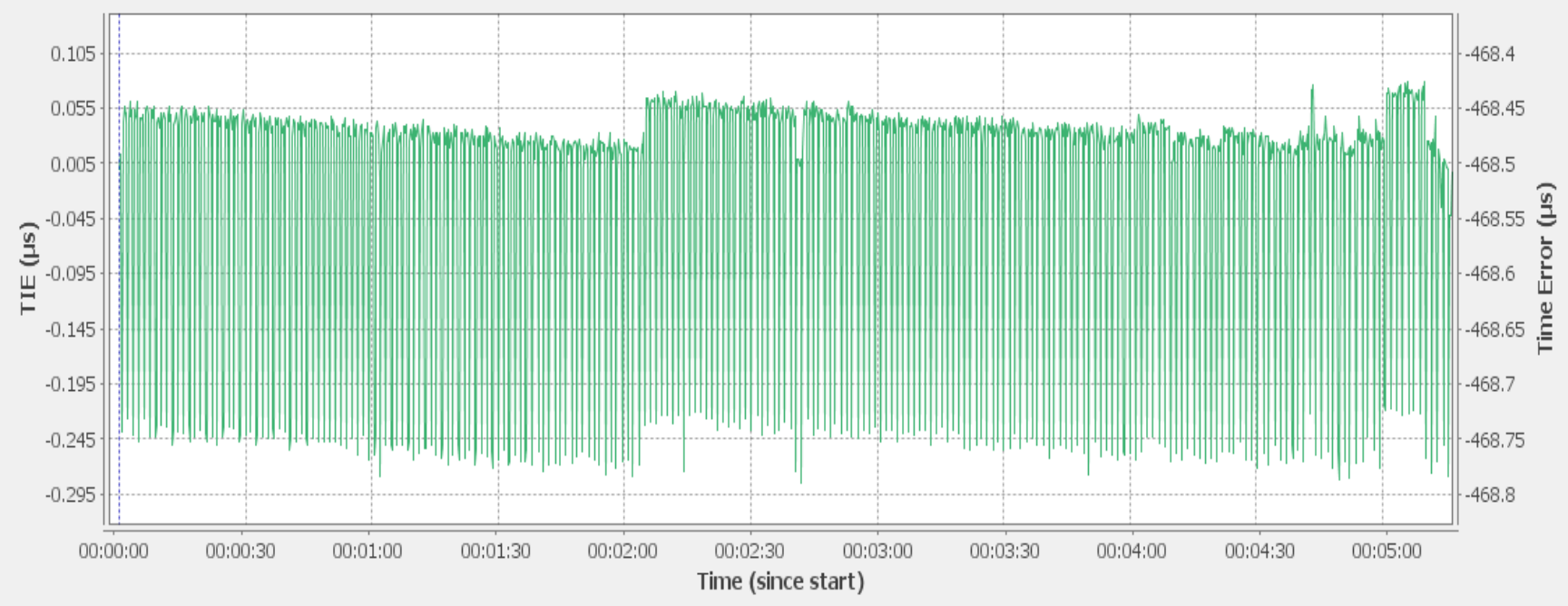
Evaluate impact of Boundary Clock's timing impairment on Slave's recovered clock

Examples of Boundary Clock Impairment

- Experiments on a real-world engineering prototype
  - The time error represented here indicates the difference between the time-stamp and the actual measured arrival time of the packet (time-stamp error)
- Changes in this impairment were observed when the conditions changed
  - Changing the sync packet rate from the Grand Master to the BC's slave port, or from the BC's master port to the slave
  - Adding background traffic to the Boundary Clock under test
  - Adding time error (impairment) from the Grand Master to the BC's slave port

Boundary Clock Impairment – BC #1

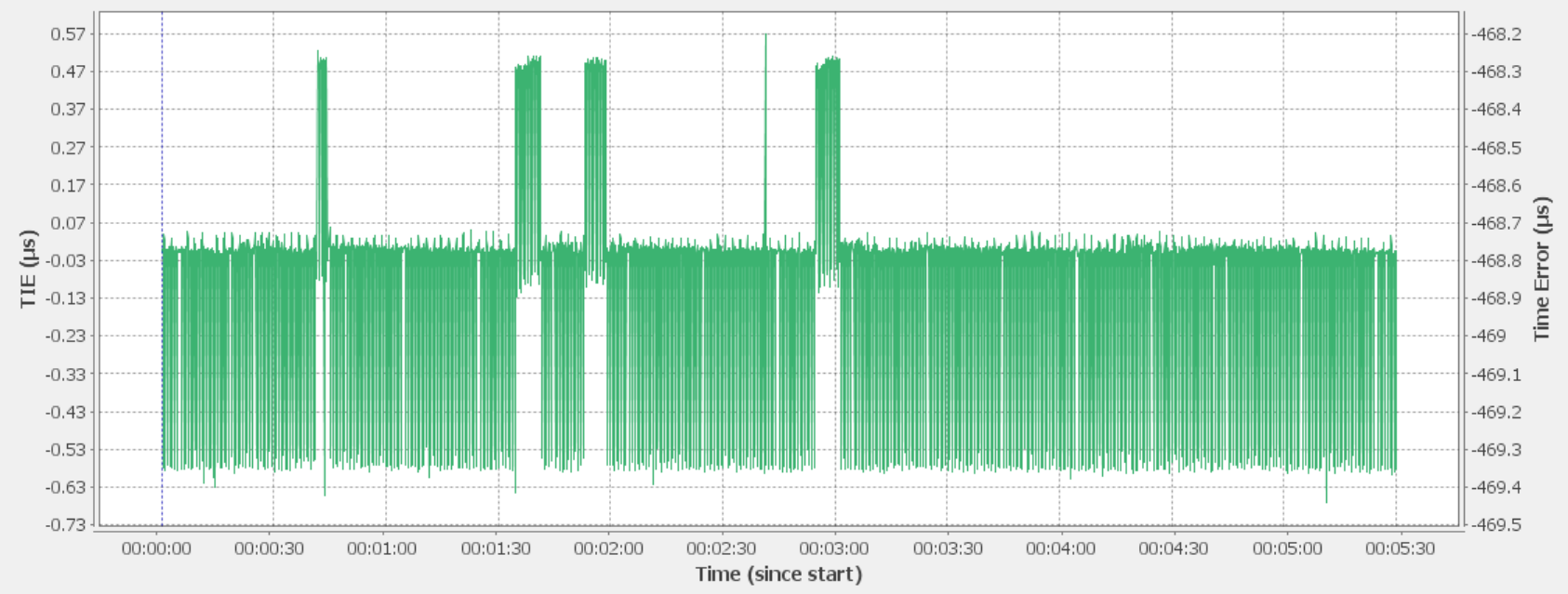
No background traffic, no impairments



- Grand Master sync rate **4pps**
- Boundary clock master-port sync rate **16pps**
- Substantial time error observed during 5-minute window

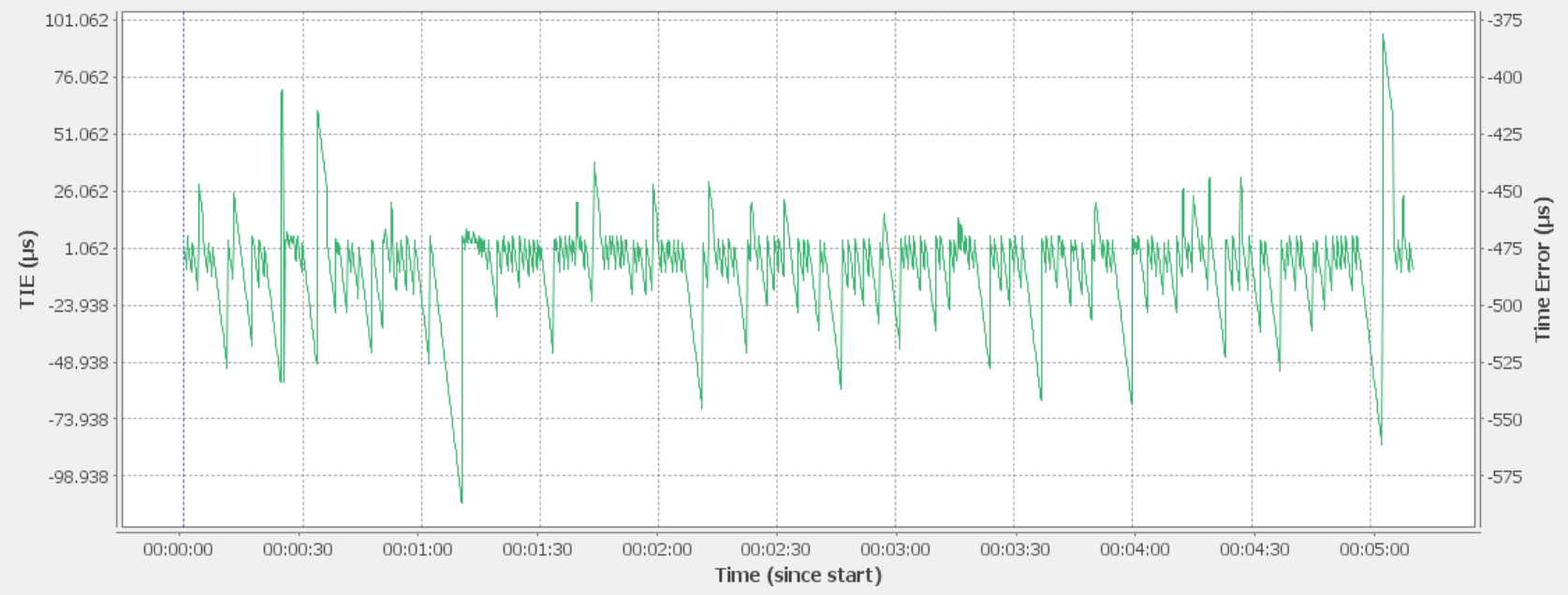
Boundary Clock Impairment – BC #1

No background traffic, no impairments



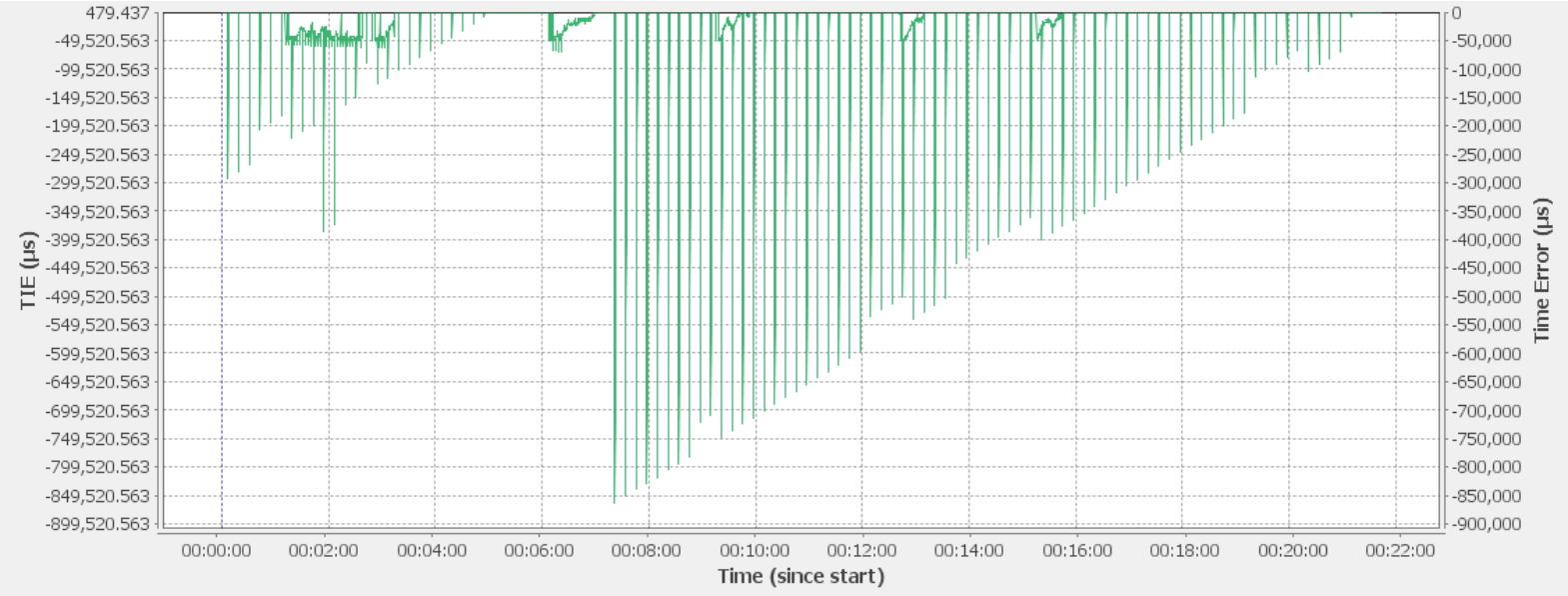
- Grand Master sync rate **8pps**
- Boundary Clock master-port sync rate **8pps**
- Dramatic change in behavior compared to other sync rate

Boundary Clock Impairment – BC #2
no background traffic, no impairments



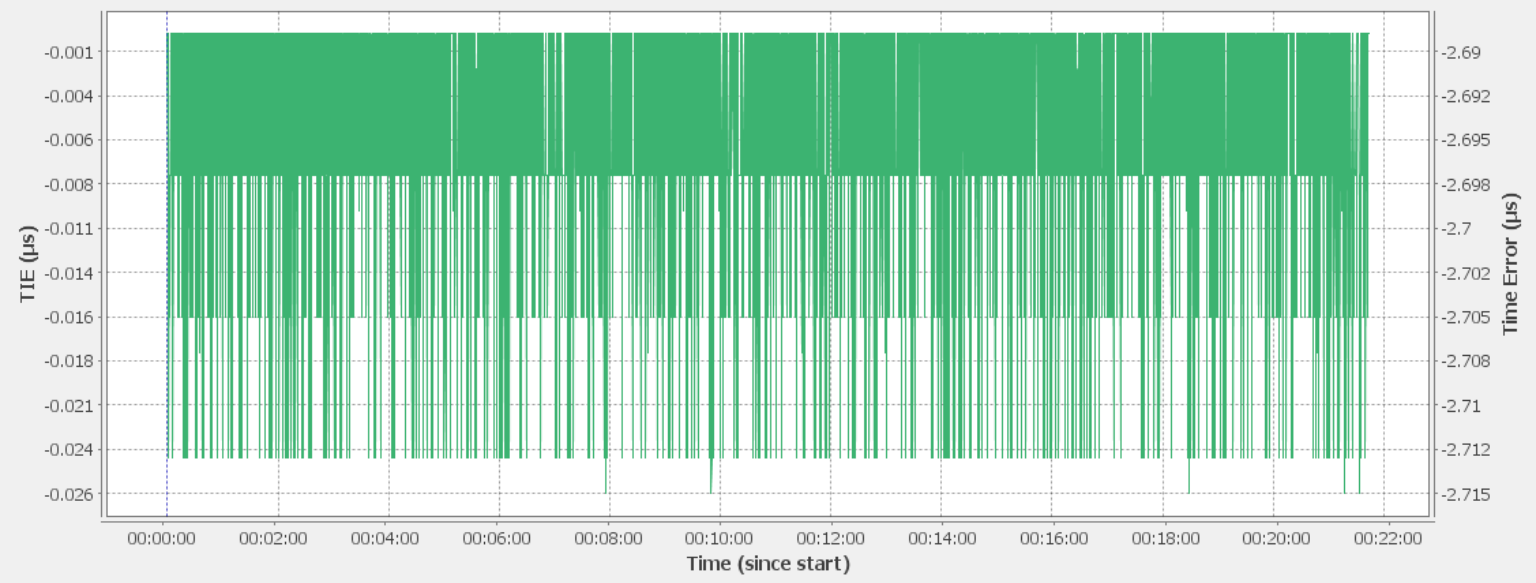
- Grand Master sync rate **8pps**
- Boundary Clock master-port sync rate **8pps**
- A different device has dramatically different results

Transparent Clock Behavior



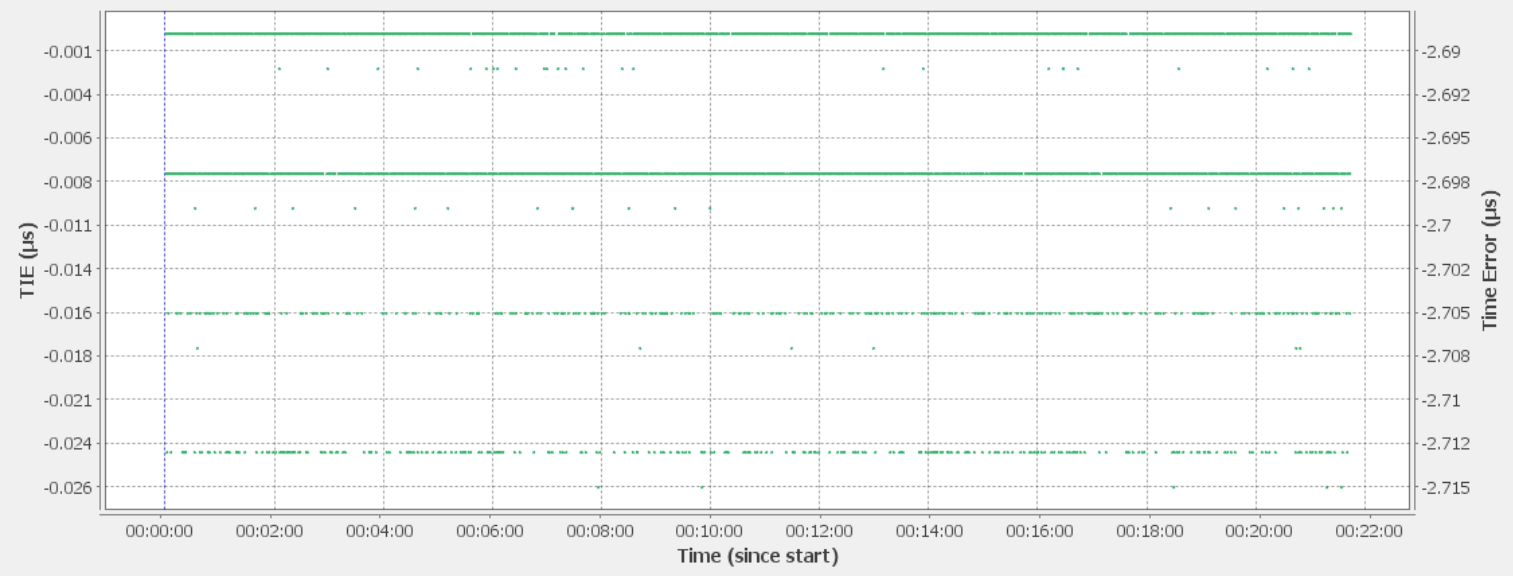
- Graph shows the “raw” delay for sync packets through the TC
- Packet delays of ~900ms were observed (even with no load)
- Grand Master sync rate **4pps**

Transparent Clock Behavior



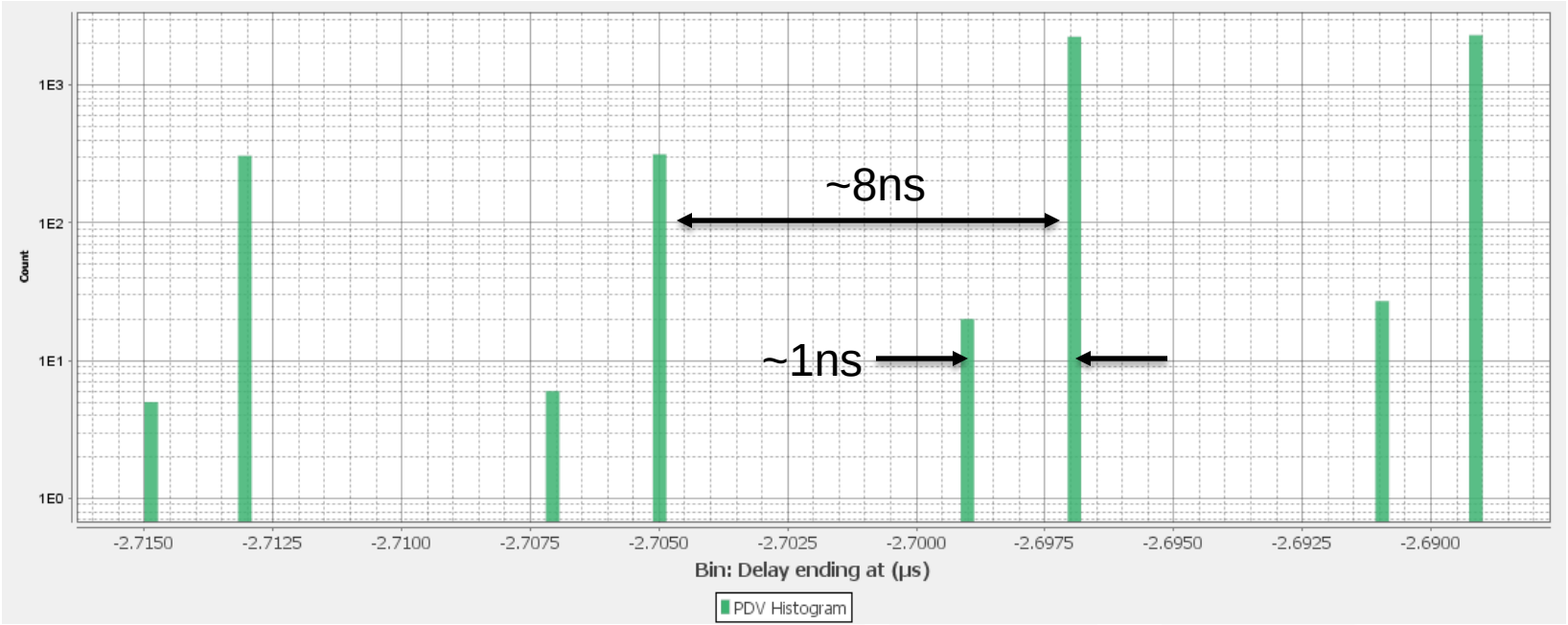
- Graph shows the corrected delay for the sync packets
- Packet delay variation reduced to ~24ns; delay error to ~2.7µs
- TC measurement granularity of 8ns is visible
- Note: this behavior was observed to be load independent

Measuring instrument Granularity



- The TC correction quantization is ~8ns
- Observation of this granularity requires test device to measure with a precision of much better than ~4ns
- The measurement granularity of the test equipment is seen to be ~1ns

Measuring instrument Granularity



- Histogram view shows the ~8ns granularity of the TC and the ~1ns granularity of the measuring instrument
- Without this granularity, the discrete nature of TC correction error would not be visible

Concluding Remarks

- Measuring time error (static and dynamic) increasing in importance
  - “Frequency” metrics (PDV) necessary but not sufficient
- Boundary clocks (and transparent clocks) are not perfect
  - Cannot chain them indefinitely
  - Effectively introduce static as well as PDV-like (dynamic) timing impairments (time error)
- Reason for impairments may be implementation dependent
  - BCs measured were affected by sync rates and traffic loads
- G.8273 Annex A and Annex B address BC/TC testing
- Testing during equipment development phase is very helpful

Thank You!
Questions?

Back-up Slides

Boundary Clock Challenges
Inaccurate Clocks

- Boundary Clocks Introduce Impairments
  - Internal Clock
    - An internal clock is derived from the PTP on the slave port of the BC in the usual manner and this local clock is used to create time-stamps on outgoing PTP traffic
    - Inaccuracy in this clock creates impairment:
      - Inaccurate time-stamps going out the master port; *time-stamp does not accurately indicate the true real time*
    - **any errors result directly in inaccuracy in the downstream clock recovery**
  - System (PHY) clock
    - The system clock or PHY clock may be asynchronous with respect to this internal PTP-derived clock
      - Any difference in these two clocks results directly in inaccurate time-stamps**, even if the PTP internal clock is perfect**

Boundary Clock Challenges Not Ordinary Switches

- Many boundary clocks are multi-function devices with many features not related to timing that compete for resources with PTP
  - L2 features such as spanning tree, VPNs, redundancy, VLANs, etc.
  - QoS – L2 & L3, different egress and ingress, marking, priority, etc.
  - Routing, Switch Virtual Interfaces, Routing Protocols, VRFs, MPLS
- Architecture of these devices may not be ideal for PTP
  - Designed primarily for fast switching of packets from port to port
  - Limited emphasis on speed, latency, etc. of CPU-generated or control-plane traffic
- These caveats of Boundary Clocks are important to characterize
  - They may not typically perform like a standard L2 switch with respect to PDV
  - They may have significant impact on the performance of PTP networks
- *A boundary clock cannot simply be treated as if it were an ordinary switch for testing purposes*

Testing Questions Remain

- Important questions remain regarding BC/TC testing
  - What limits or metrics are applicable for impairment introduced by a boundary clock as in Test Scenario #1?
    - TIE / PDV? Maximum Time Error? What limit is to be expected?
    - Will require both: *constant time error* (“static”), as well as TIE/PDV (“dynamic”)
  - What PDV impairment profiles apply to test with impairments before and after the Boundary Clock as in Test Scenario #2?
    - Does some model apply which emulates *N* number of Boundary Clocks, or networks combining Boundary Clocks with ordinary switches?
  - What is the precision/accuracy required in the test equipment?
    - Rule-of-thumb: at least one order of magnitude better than the same function in the DUT (e.g. time-stamping)
    - Test signal generation (e.g. introduction of wander):

Testing Challenges
Boundary Clock as Slave or Master

- Testing Boundary Clock as a slave or ordinary clock
  - Many Boundary Clocks do not have recovered clock interfaces to measure
  - The standard G.8261 tests are performed without regard for the Boundary Clock's master port behavior, therefore do not address the purpose of the boundary clock
  - This test does not address the time impairment introduced by circuitry between the boundary clock's slave and master ports
- Testing Boundary Clocks as a master clock
  - The standard G.8261 tests are performed with PDV impairment is added between Boundary Clock and slave. Slave's recovered clock interface is evaluated against the standard MTIE/TDEV masks
  - This test does not address the ability of the Boundary Clock to recover an accurate clock in the presence of time error between the BC and the GM
  - The Boundary Clock is not being measured directly; the result is dependent on the performance of the slave device

Boundary/Transparent Clock Testing
Suggested Best Practices

- Monitoring/measuring time error on both sides of a boundary/transparent clock
  - Comparison between input and output reveals the static and dynamic impact of the device and we can verify whether it is affected by
    - Background traffic, incoming and outgoing sync packet interval, QoS, routing, etc
- Impairment on both sides of a boundary/transparent clock
  - Impairment is added between the GM Clock and BC/TC, and between the BC/TC and slave clock, simultaneously; recovered clock at remote slave is measured
    - Profiles need to be developed
- Measure ToD error and phase (1PPS) error introduced by boundary clocks
  - Monitor and measure timestamp accuracy of sync, follow-up packets from master port of boundary clock and measure phase offset of 1PPS between GM Clock and Slave with boundary clock inbetween