Power Matters

A Look at SyncE and IEEE 1588

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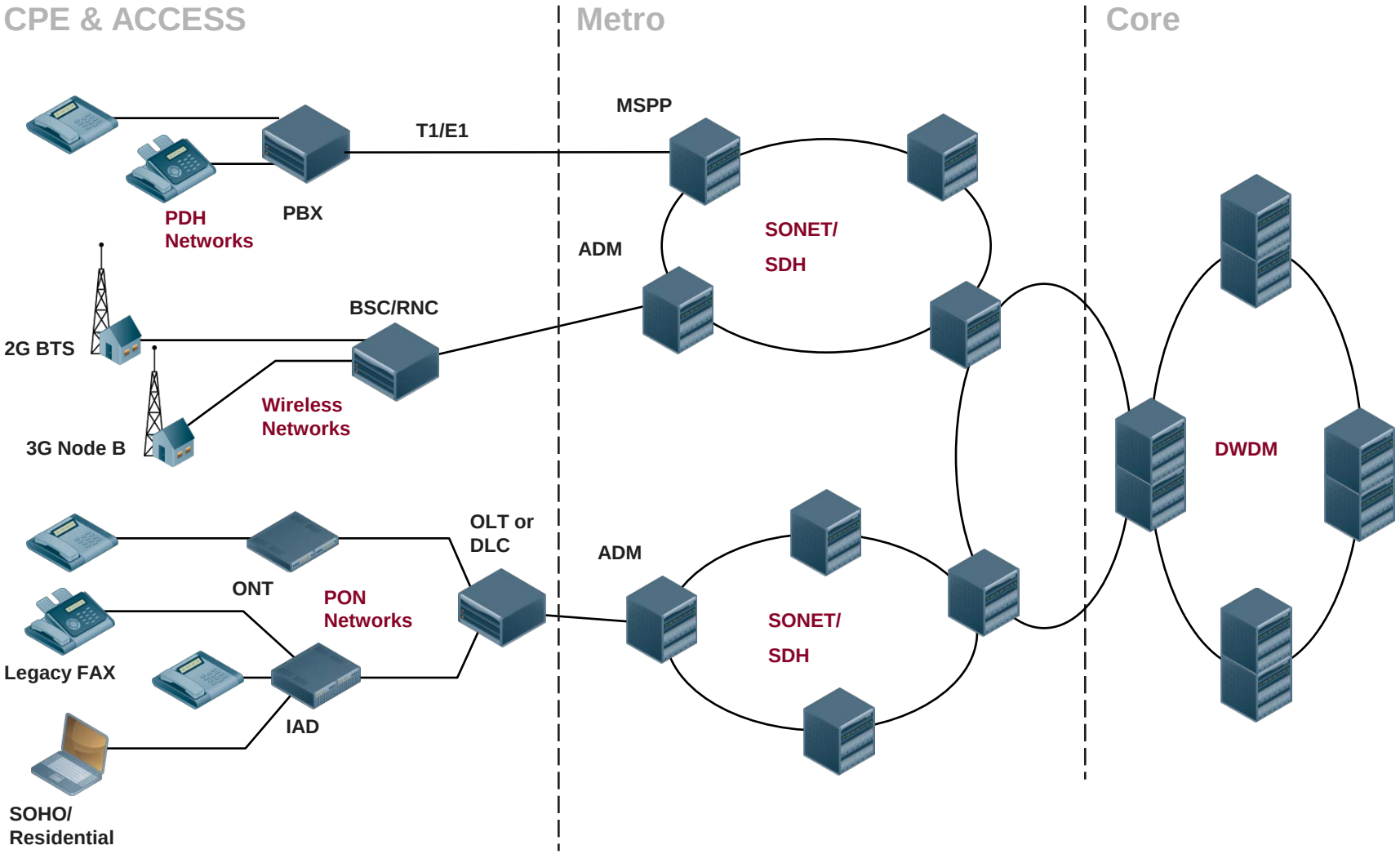
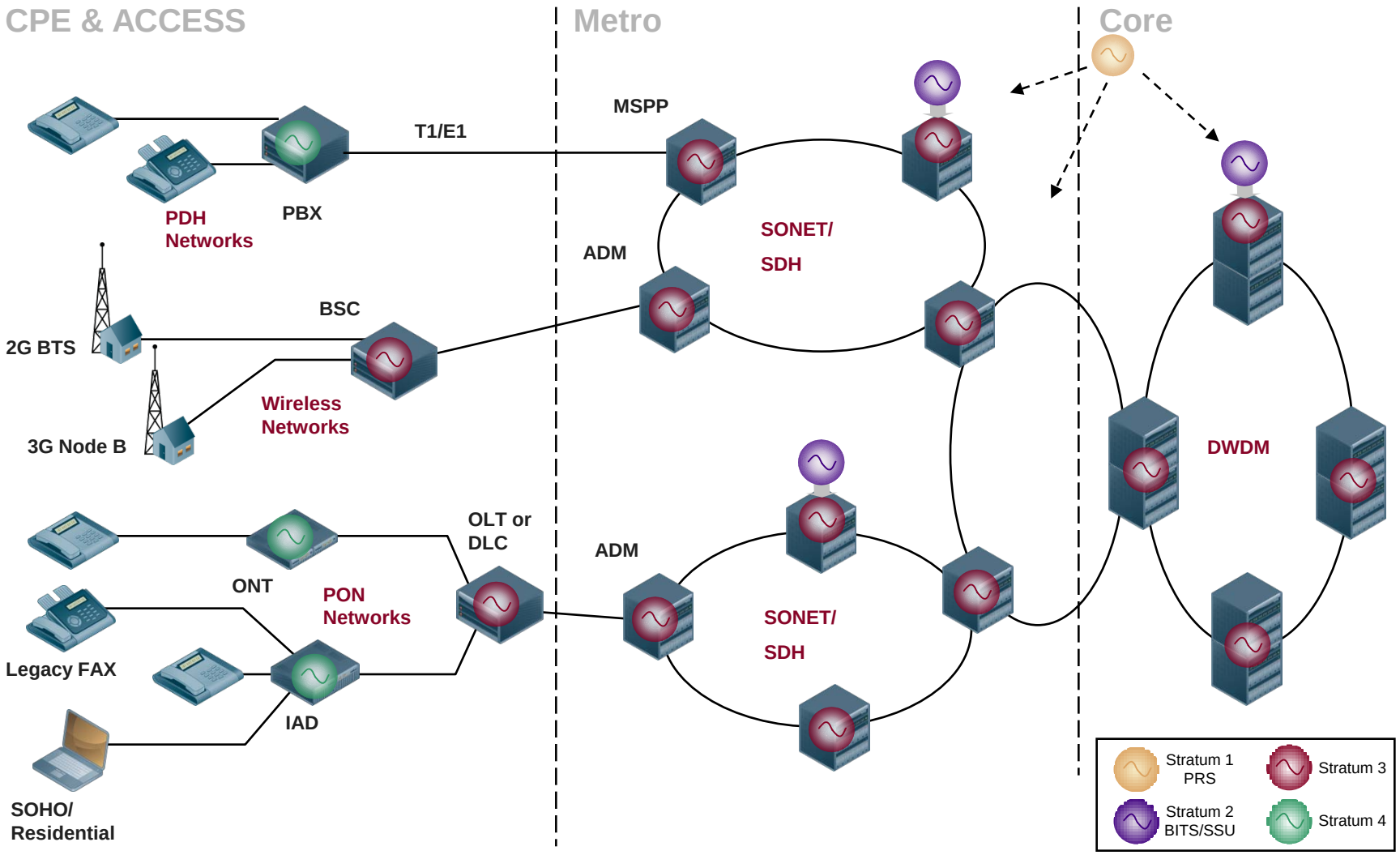
Generic Circuit Switched Network Diagram - Where is the Synchronization?

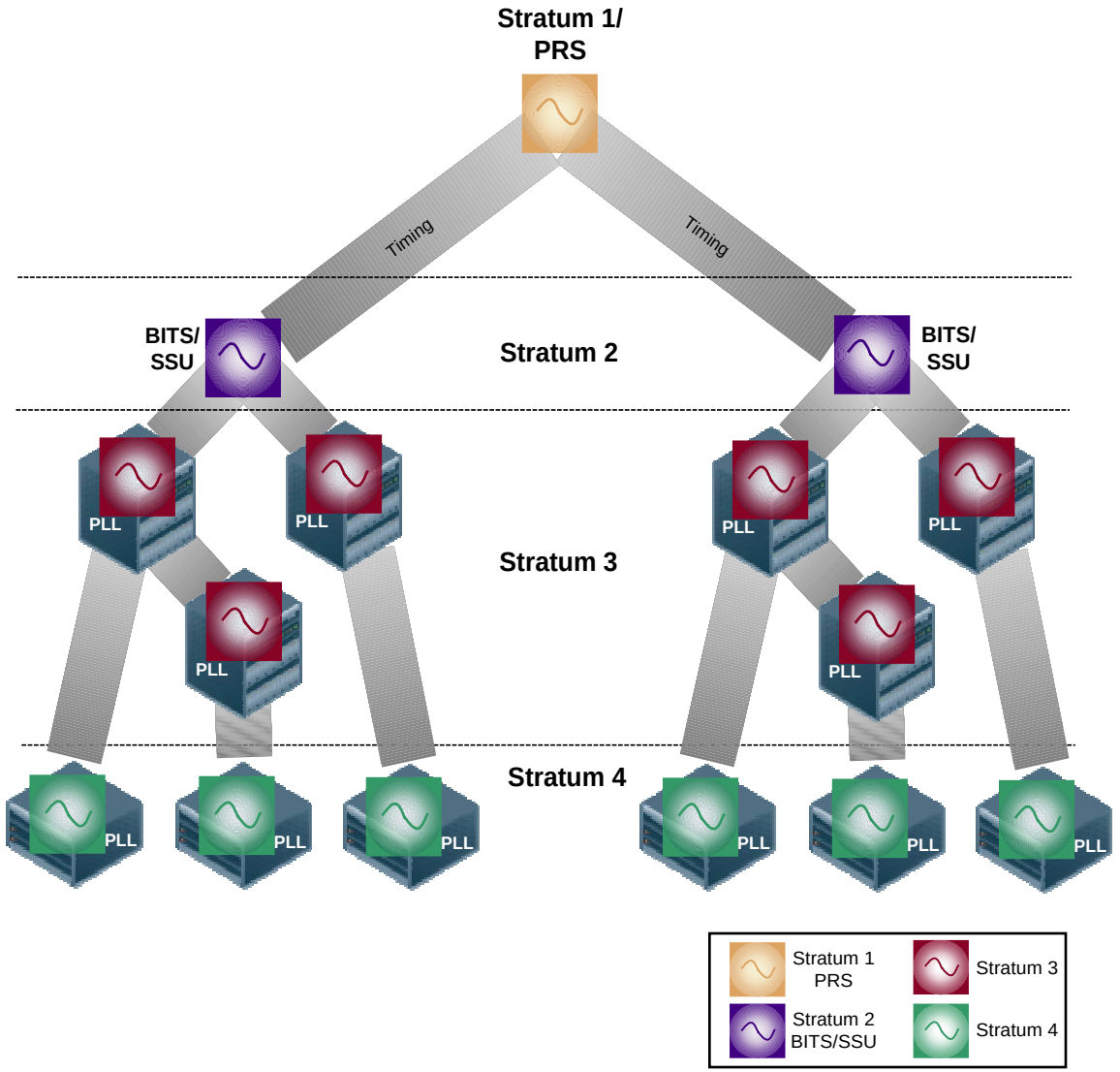


Generic Circuit Switched Network Diagram - Found the Synchronization

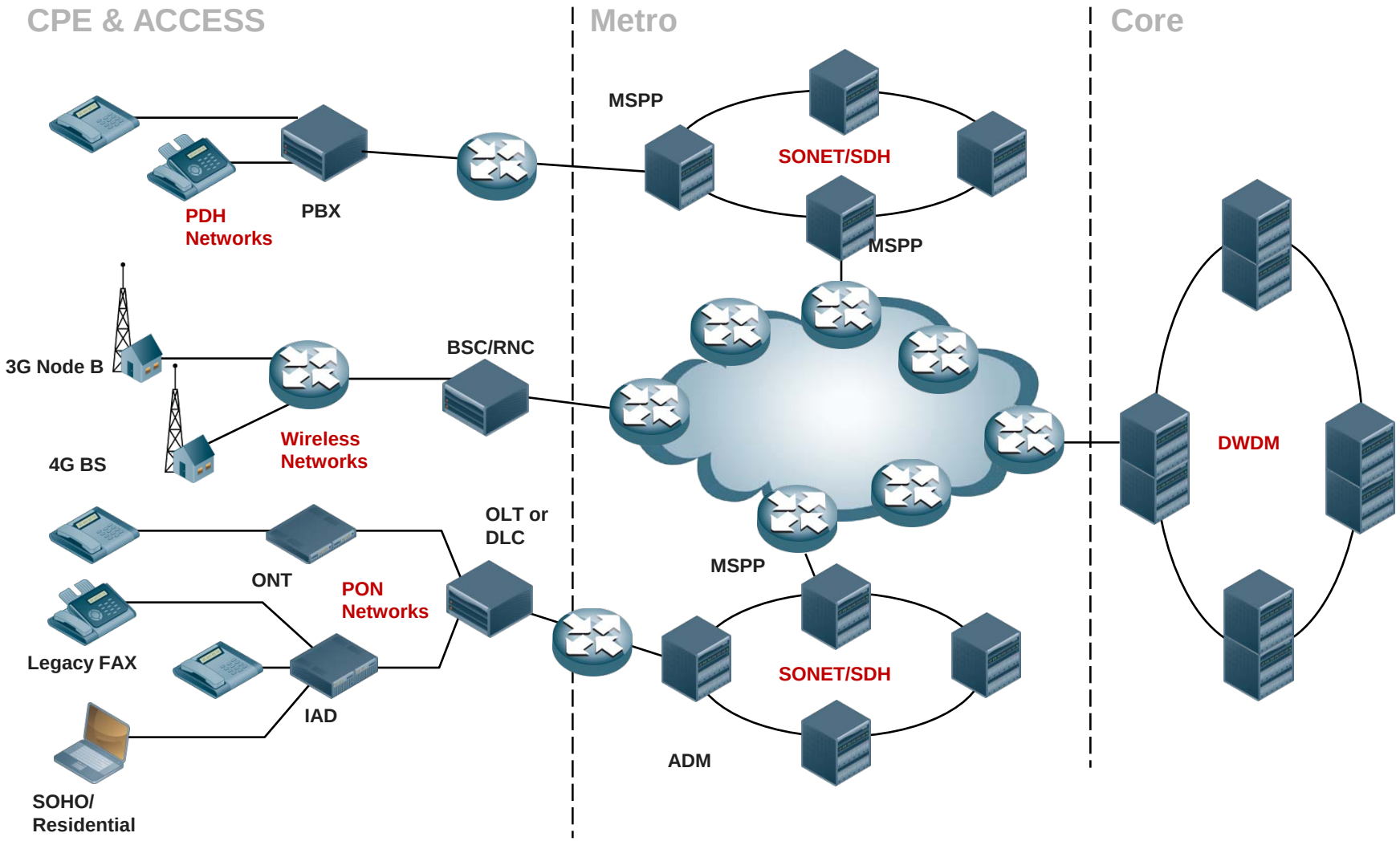


Re-organizing the Synchronization into a Logical Flow

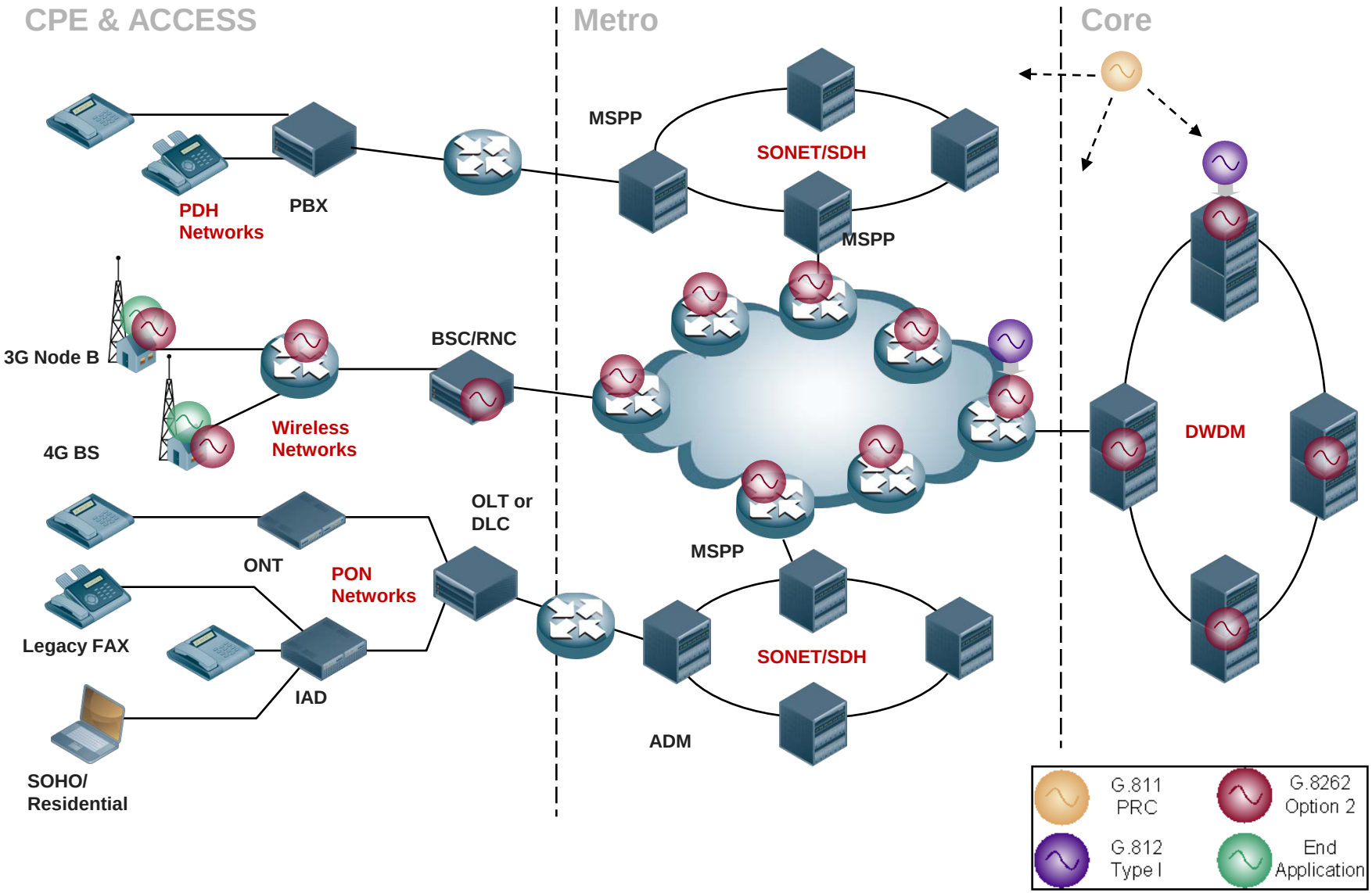
- A Stratum 1 clock (or PRS) provides a highly accurate reference for the entire network
- Stratum 1 provides the highest level of frequency accuracy followed by the Stratum 2, the Stratum 3, and the Stratum 4
- PLLs synchronized to the PRS are used in the timing distribution chain to “transfer” the PRS’s frequency accuracy throughout the network
- In the case where a PLL in the timing distribution chain is isolated (not synchronized to the PRS), it generates timing at its own frequency accuracy



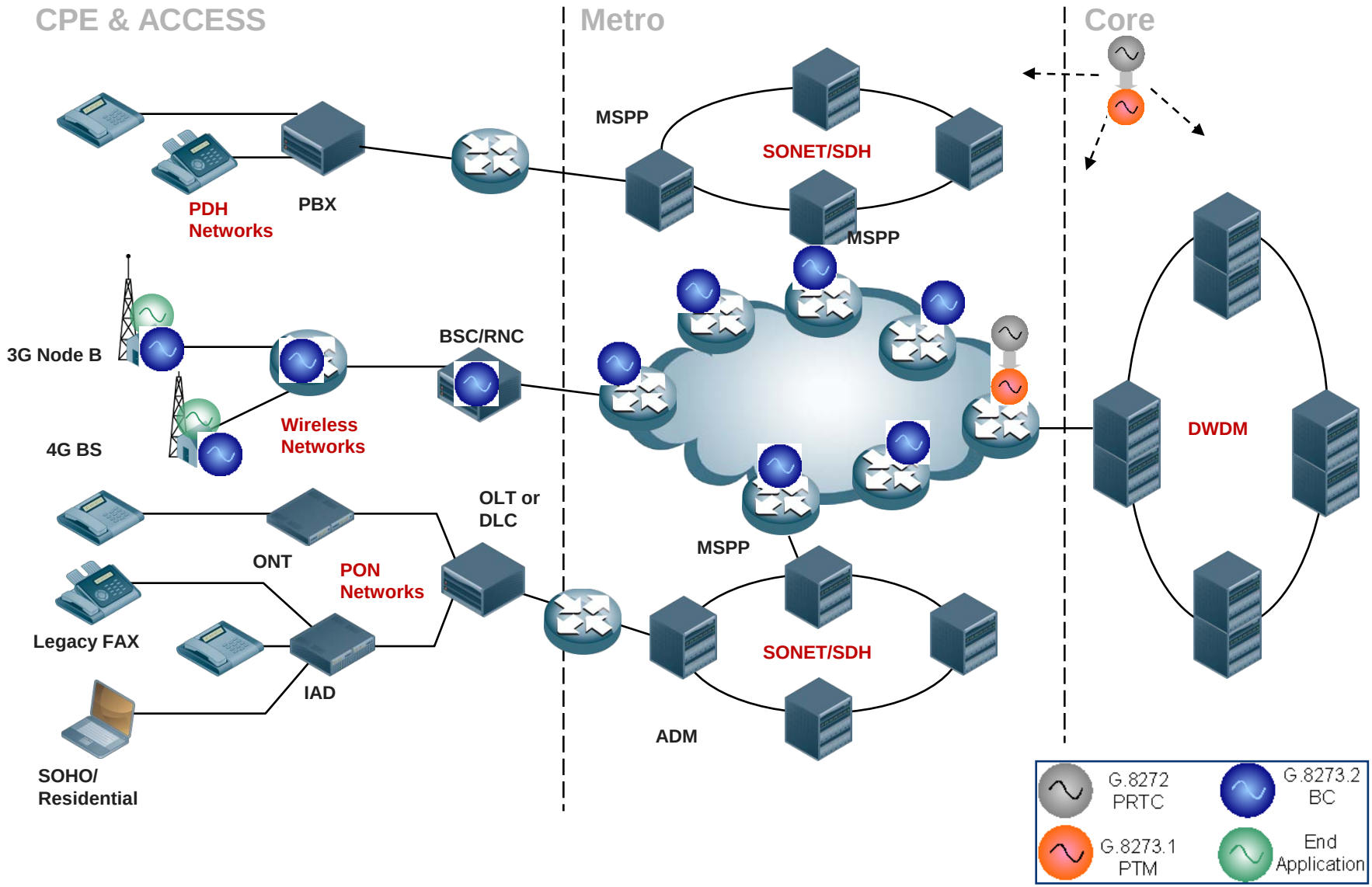
Generic Packet Switched Network Diagram - Where is the Synchronization?



Found the Wireless Backhaul Clock Chain - Physical Layer Synchronization

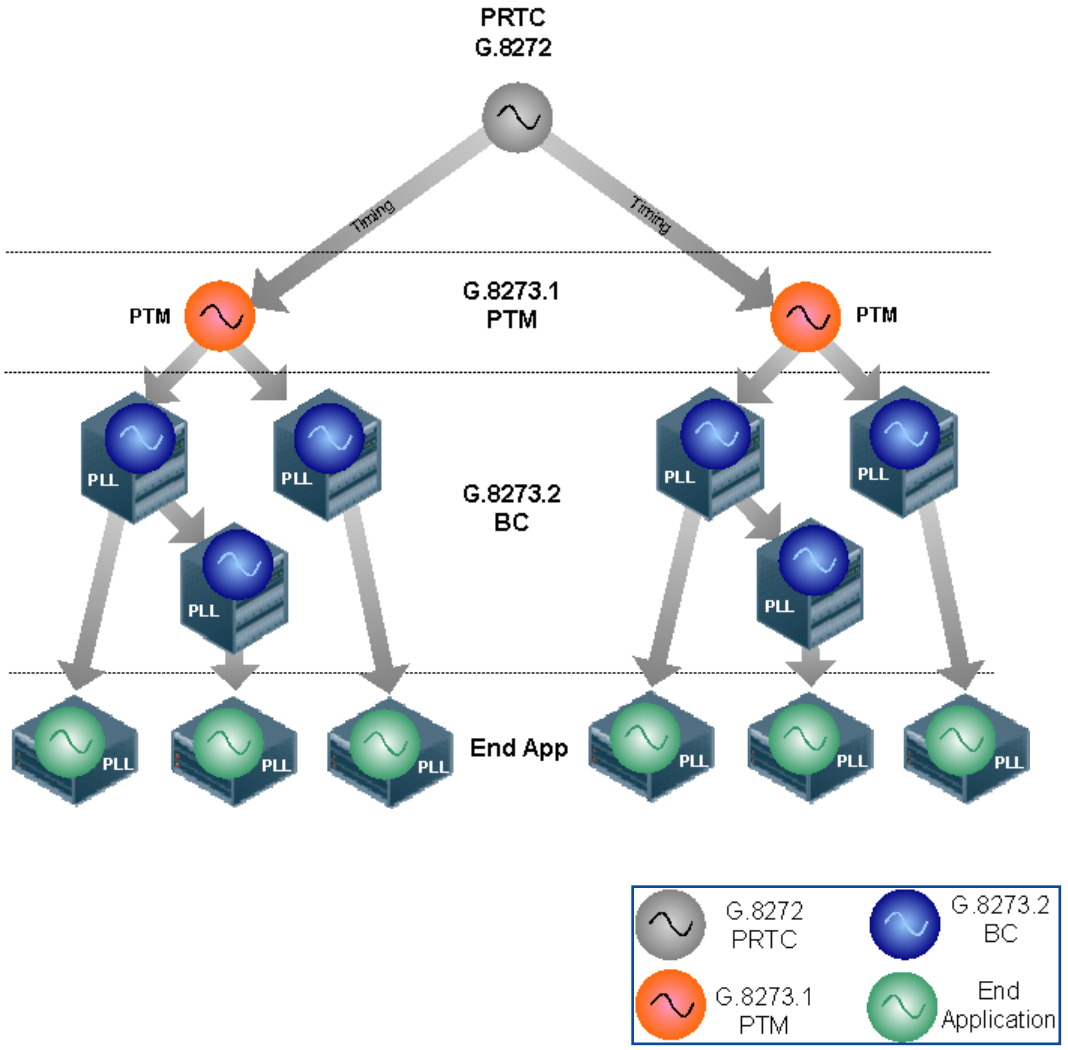


Found the Wireless Backhaul Clock Chain - Protocol Layer Synchronization

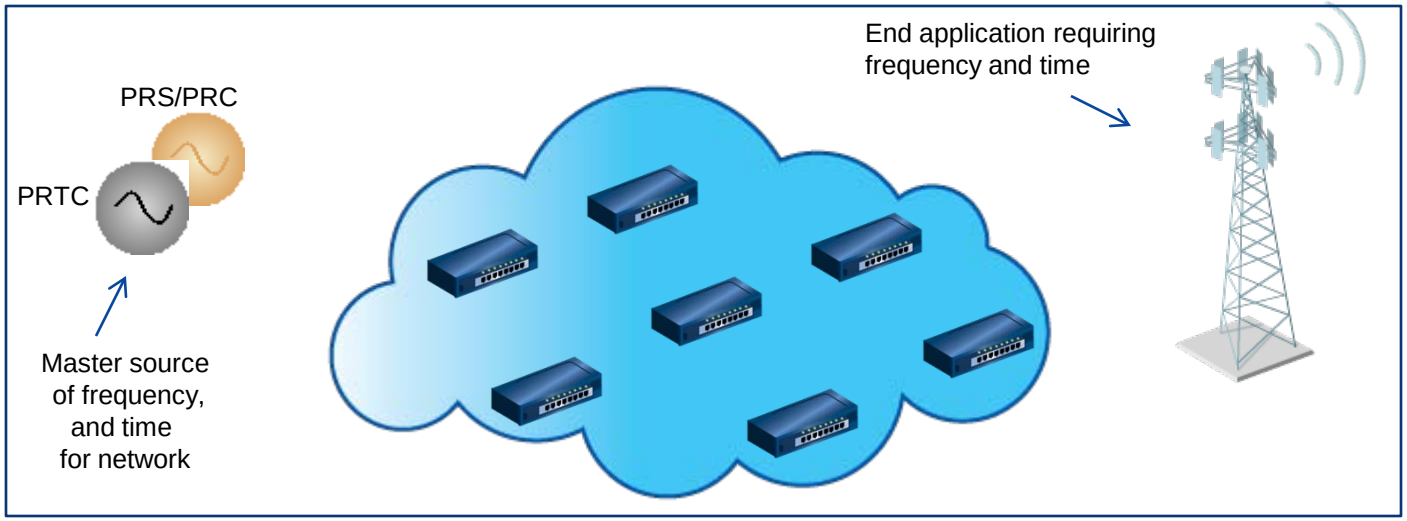


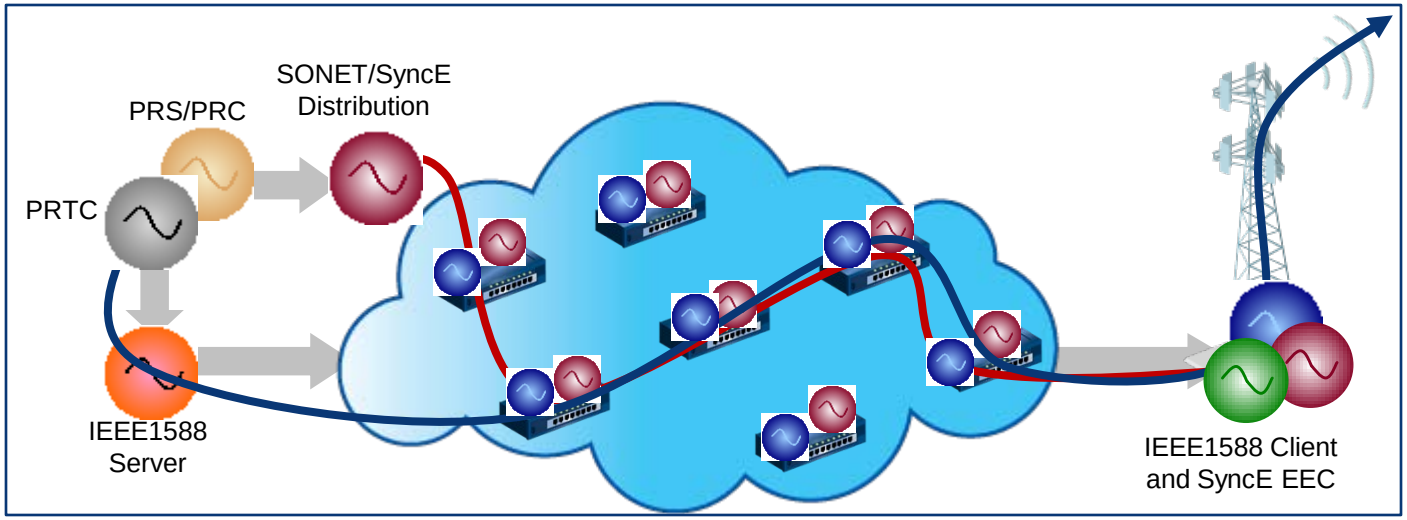
Re-organizing the Synchronization into a Logical Flow

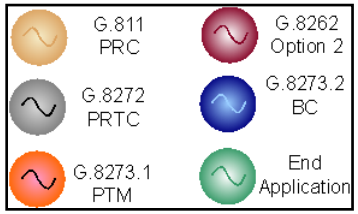
- A PRTC provides a highly accurate time of day reference for the entire network
- A PTM distributes the time of day using IEEE 1588-2008 protocol
- A BC synchronizes itself to an upstream PTM or BC, and additionally propagates synchronization downstream to the next BC
- The end application may have its own unique requirements for synchronization, employing its own synchronization clock type



Combine Physical Layer & Protocol Layer Synchronization into a Single View

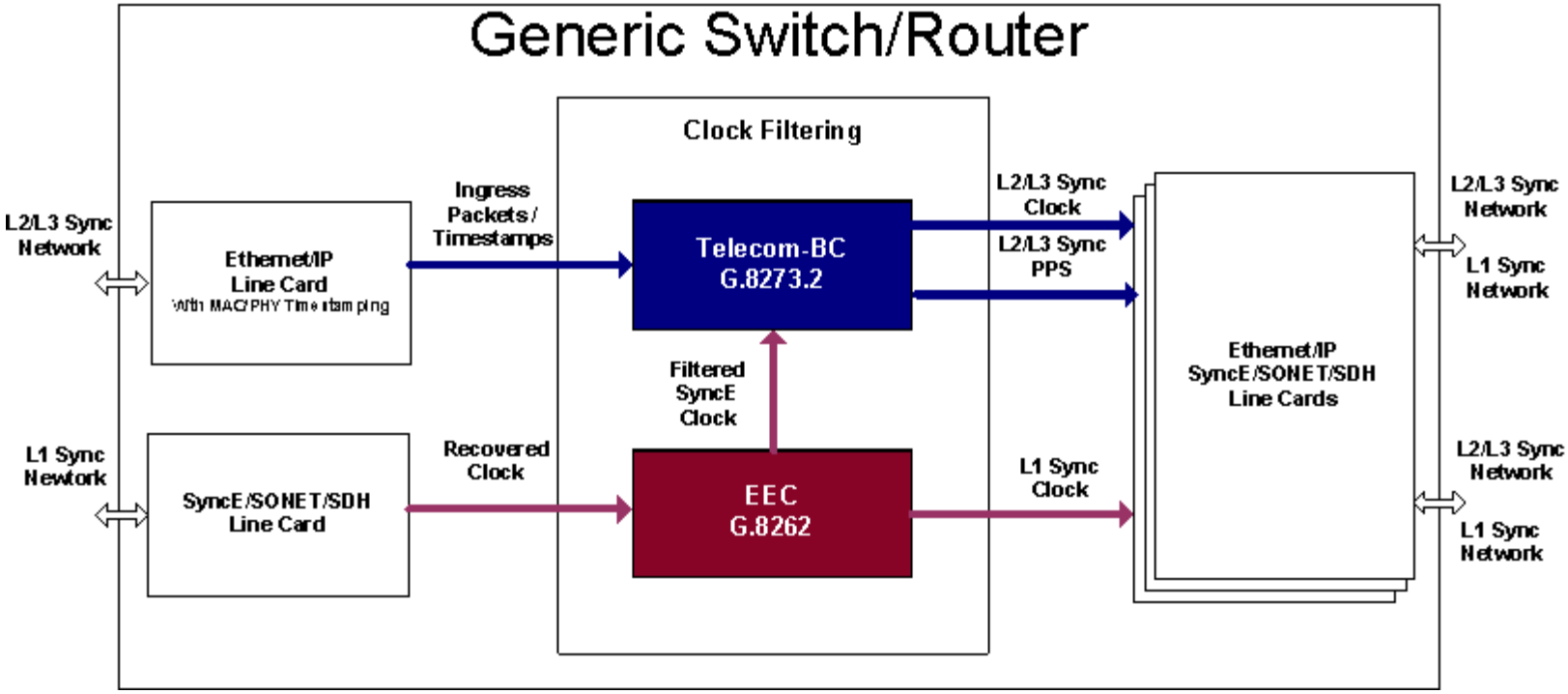






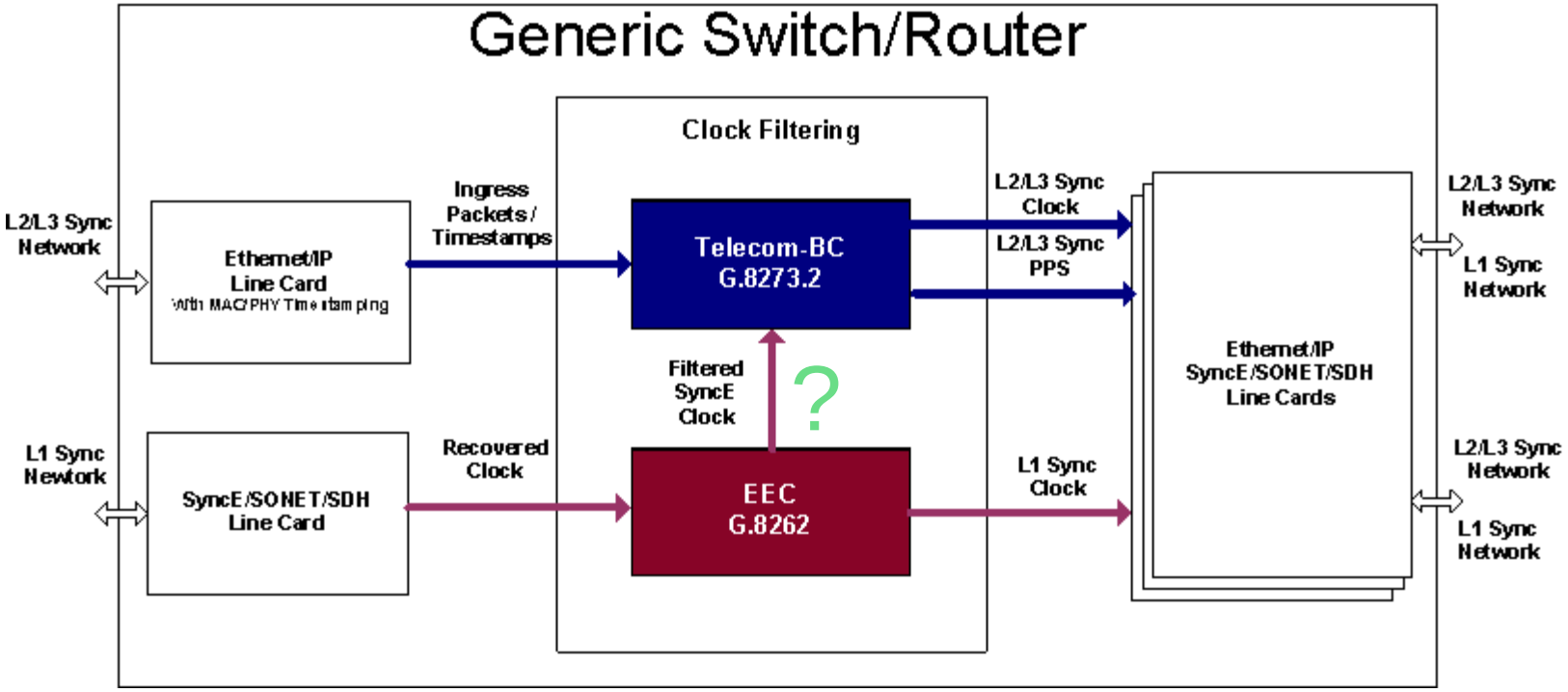
Zoom Inside a Generic Switch/Router with Multiple Line Cards & Timing Cards

- Physical layer synchronization path implements G.8262 EEC functionality
  - Option 1 Europe/China/India, Option 2 USA/Japan
  - Unaffected by protocol layer synchronization path – the IEEE 1588 BC does not impact the SyncE/SDH reference chain (e.g. lock time, wander transfer)
  - This path exists today in the SyncE, SONET/SDH, PDH reference chain
- Protocol layer synchronization path implements G.8273.2 Telecom Boundary Clock
  - Uses the filtered physical layer synchronization clock from the EEC



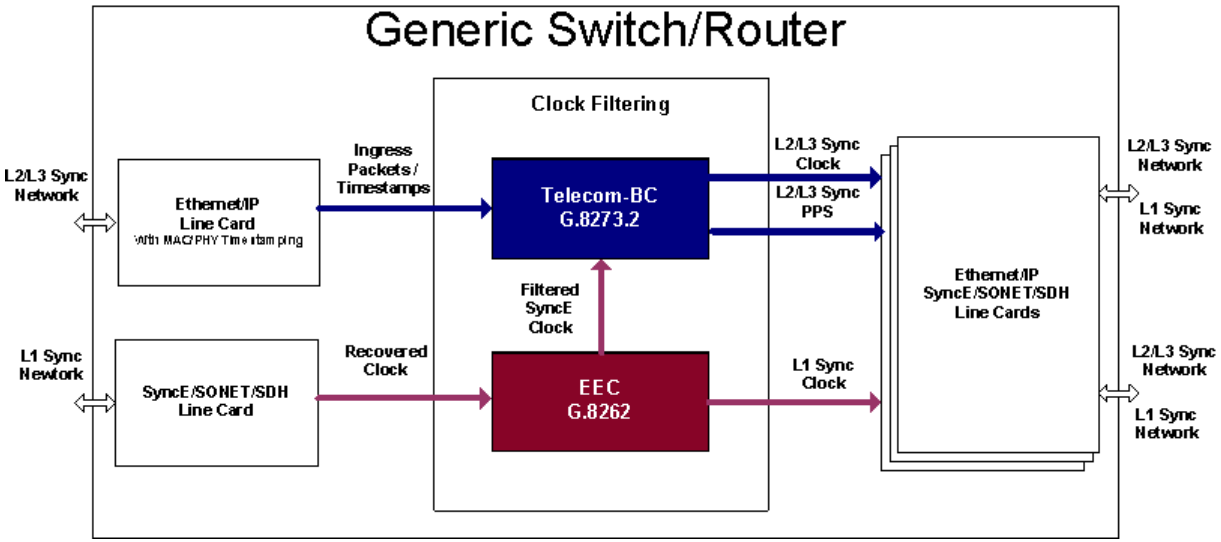
What's that line between the EEC and T-BC?

- Telecom Boundary clock uses the SyncE clock from the EEC for syntonization
- This is different than a traditional PLL, where there is normally only one source of information active concurrently
- If a highly reliable physical layer clock (SyncE, SONET/SDH, PDH) is not present then the Telecom-BC can operate without physical layer syntonization, too



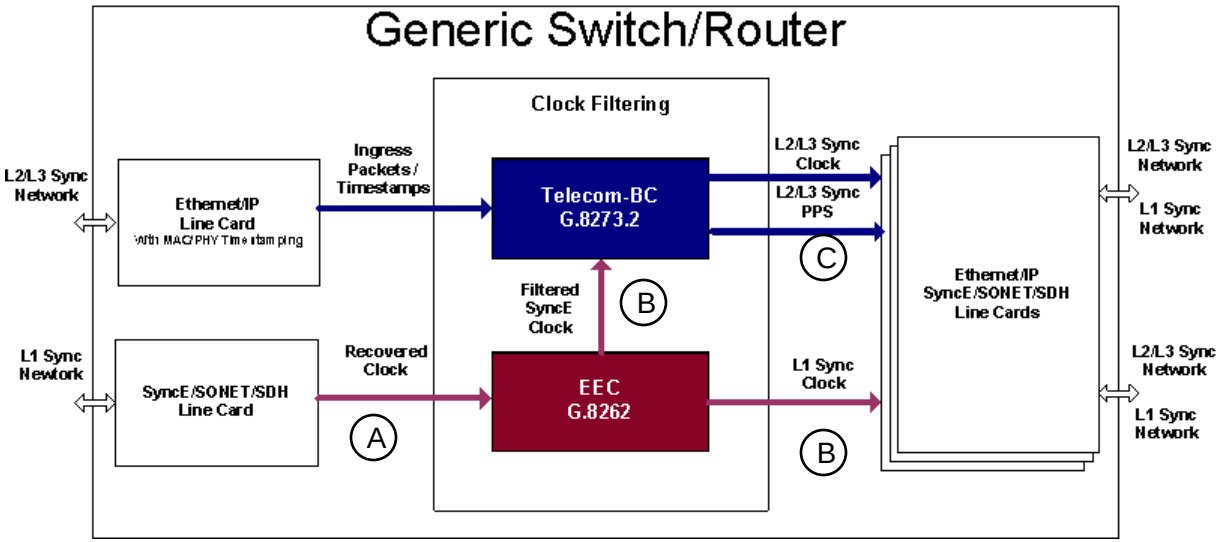
Telecom Boundary Clock using SyncE

- The SyncE clock is traceable to PRC/PRS with 10^-11 accuracy (0.01 ppb) or better, whereas IEEE 1588 is normally traceable to a GNSS (e.g. GPS)
  - Phase accumulation is < 10 ns over 1000 seconds (15 minutes)
  - Phase accumulation will be corrected by the IEEE 1588 phase algorithm, when needed, smoothly through the BC filter
    - Applies both to networks with BC in every node where corrections may be every few minutes (errors < 8 ns may not be visible due to resolution on timestamp insertion/recording) and networks with some BC and some unaware elements where correcions may be much less frequent due to low bandwidth of the IEEE 1588 algorithm
- The SyncE clock stability far exceeds a replacement oscillator for this type of application
  - Common TCXOs for a T-BC would have a maximum drift of 320 ppb/day. These TCXOs would be similar to oscillators for SONET/SDH with an bandwidth of 100 mHz



Telecom Boundary Clock using SyncE

- Disturbances on the physical layer clock may be handled with two-stage approach
  - These may be the result of an upstream reference switch
  - Modern PLL reference switching is 'hitless', meaning no noticeable impact on TIE
- The input disturbance that must be tolerated (but is not necessarily present) by the EEC is at point A
- The EEC minimizes the impact of this disturbance according to specific criteria in G.813/G.8262, based on bandwidth, gain peaking and phase slope limiting and the output after such handling is seen at point B
- The Telecom-BC then may act as a second stage transient suppressant, with advanced capability and combining with the phase information from IEEE 1588 produce an output clock at point C
  - Noting that G.8262 is built on legacy G.813 specification from many years ago, before common techniques like phase build-out were available to handle transients



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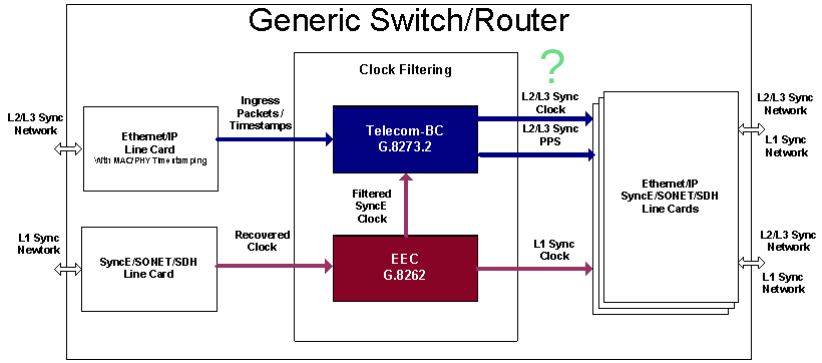
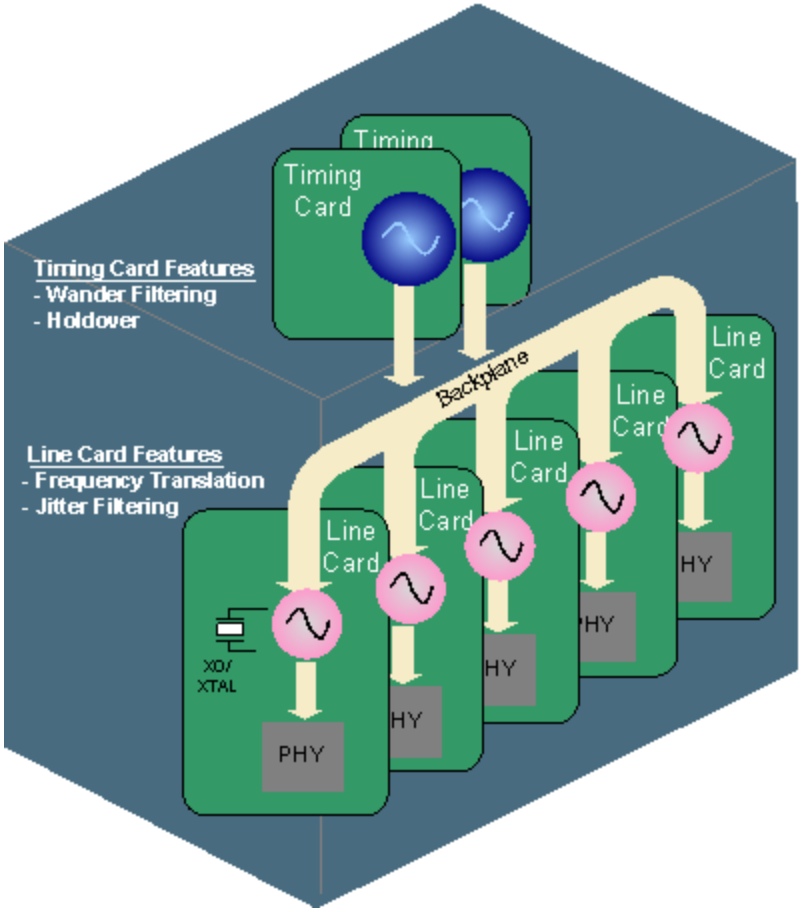
Why does the Telecom-BC provide both PPS and Clock to the Line Cards?

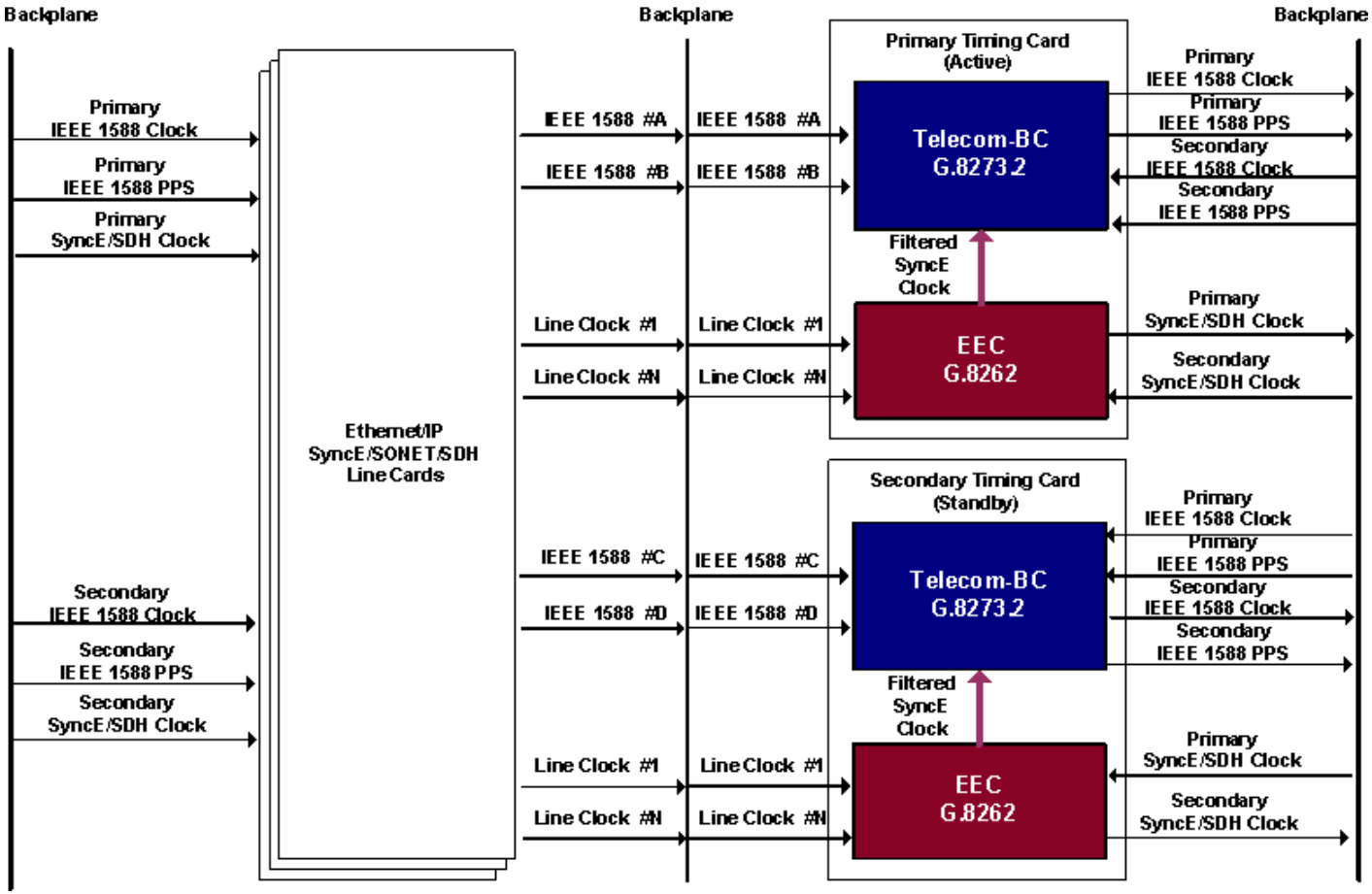
- On the line card there is normally a PLL that is responsible for frequency translation (rate conversion) to drive very low jitter clocks to the Switch/PHY components
- If the PPS and Clock are both provided over the backplane, this PLL bandwith may be wide and may use a low cost crystal
- If the PPS only is provided, a bandwidth generally < 100 mHz must be used to synchronize and rate covert to a higher frequency, such as 10 MHz
- Summary: Telecom BC provides the PPS and Clock so that each line card cost can be substantially reduced!





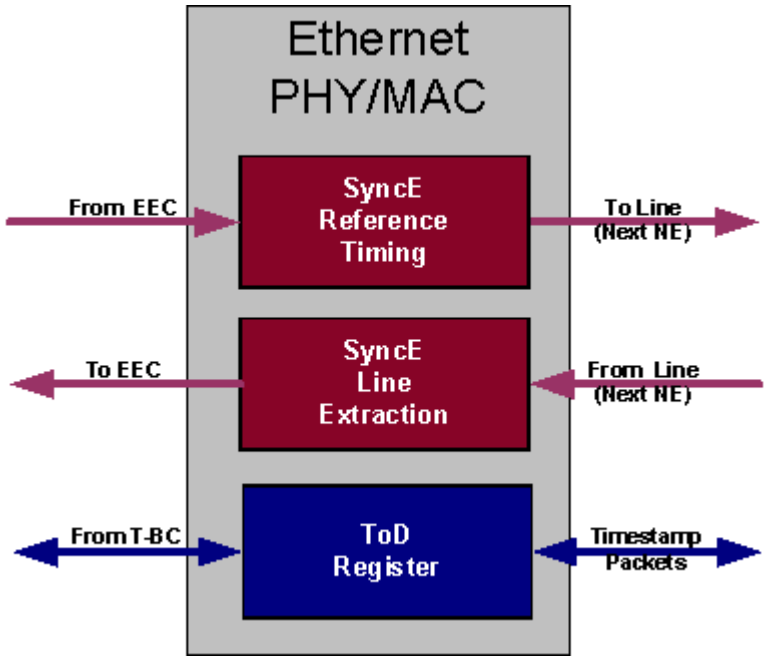
Timing Card Redundancy

- Redundancy normally implemented using an active and standby timing card
  - Note this card may not be dedicated only to synchronization, but likely resides on a controller card (which itself has similar redundancy needs)



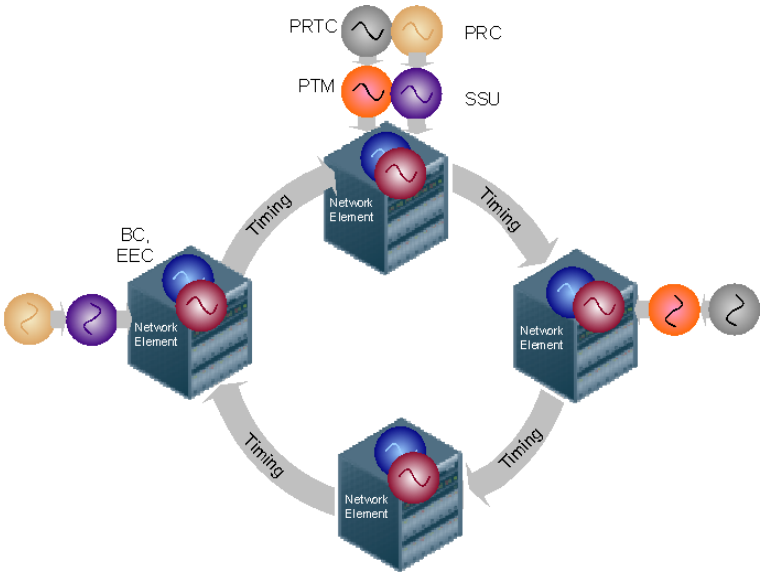
Line Card Functionality

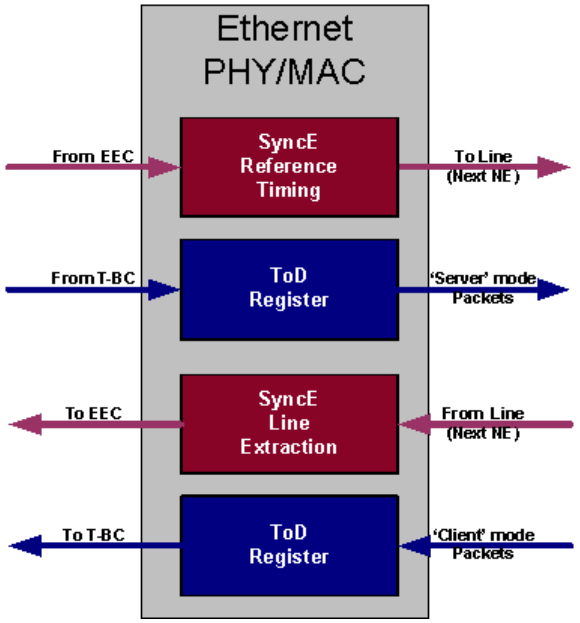
- Ingress SyncE clock extraction from the line
  - Provided to EEC
- Synchronize to a reference clock to drive SyncE egress on the line
  - Provided from the EEC
- Identify & timestamp packets using a reference clock & PPS
  - Reference clock & PPS may be provided by Telecom-BC
  - Timestamps generated from Time-of-Day inside component, set/adjusted by Telecom-BC



Anything special I may need to consider? Ring architectures / Full Duplex

- So far, selection of PHY component includes
  - Timestamping capability
  - Ingress SyncE clock extraction
  - Egress SyncE clock timing from reference sync
- SyncE timing in PHY independent today for ingress and egress direction
  - (Excluding 100 Mbps, 1 Gbps copper)
- IEEE 1588 timing in PHY uni-directional
  - Use Announce to figure out if should be 'Server' mode (providing timing egress) or 'Client' mode (locking to timing ingress)





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Thank-you for your time and attention