Implications of Timing in Telecommunications

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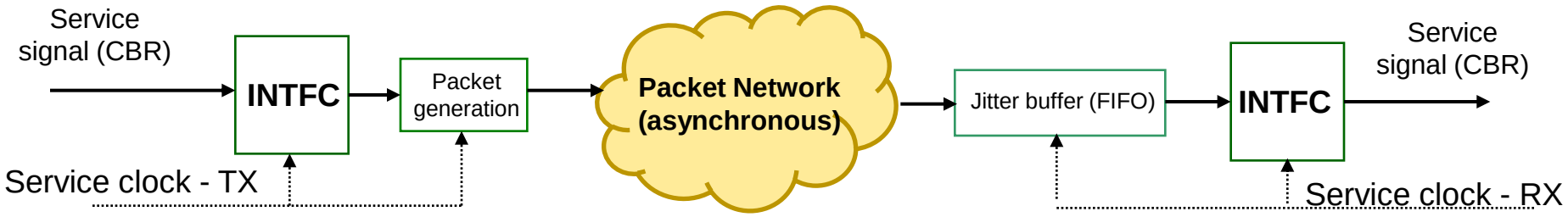
Outline of Presentation

- Timing Alignment is Fundamental in Telecommunications
  - Digital transmission requires symbol-timing alignment
  - Digital network require synchronization to emulate analog channels
  - Circuit Emulation (CBR over packet) requires timing alignment
  - Wireless (Cellular) requires timing alignment
  - Multimedia requires timing alignment
- Timing in Circuit-Switched (TDM) Networks
  - Synchronous time-division multiplexing
  - The synchronization network
- Timing in Next Generation Networks
  - Impact of packet delay variation (PDV)
  - Testing packet-based timing transfer methods
  - Monitoring packet-switched networks

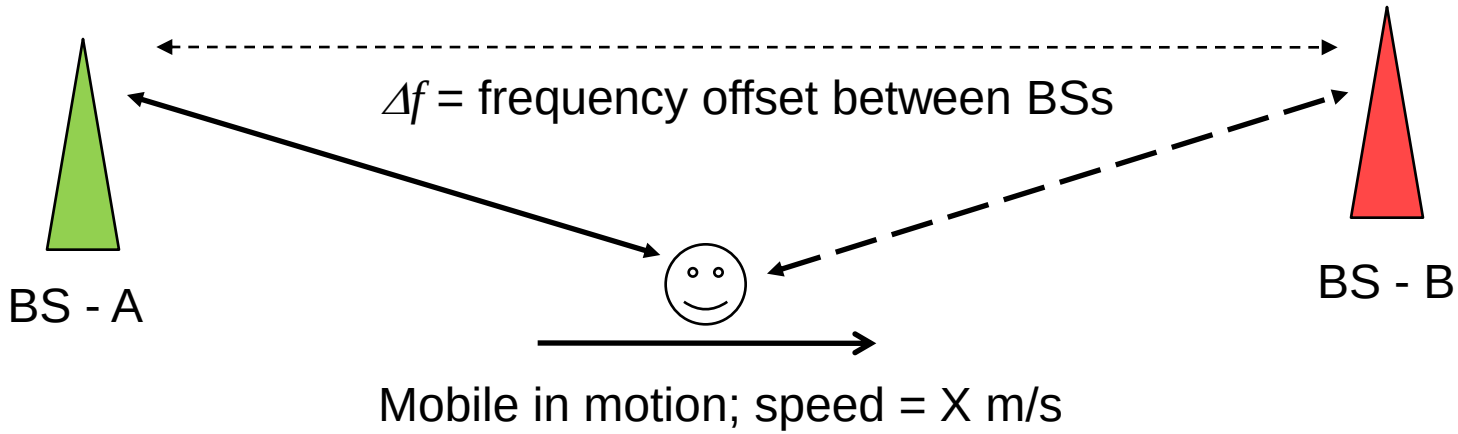
Back-up slides available

Timing alignment implicit in Circuit Emulation



- Network impairments: delay, packet-delay-variation (PDV), discarded packets
- Jitter buffer size: large enough to accommodate greatest (expected) packet-delay-variation. Packet loss concealment is not an option.
- Causes of packet "loss":
  - Network drops packets (bit errors, congestion)
  - Jitter buffer empty/full (excessive packet-delay-variation)
- Key to ***Circuit Emulation*** :
  - Ensure packet loss is (essentially) zero.
  - Make RX and TX service clocks "equal".
  - Note: If RX ≠ TX then jitter buffer is going to overflow/underflow

Timing Alignment in Wireless

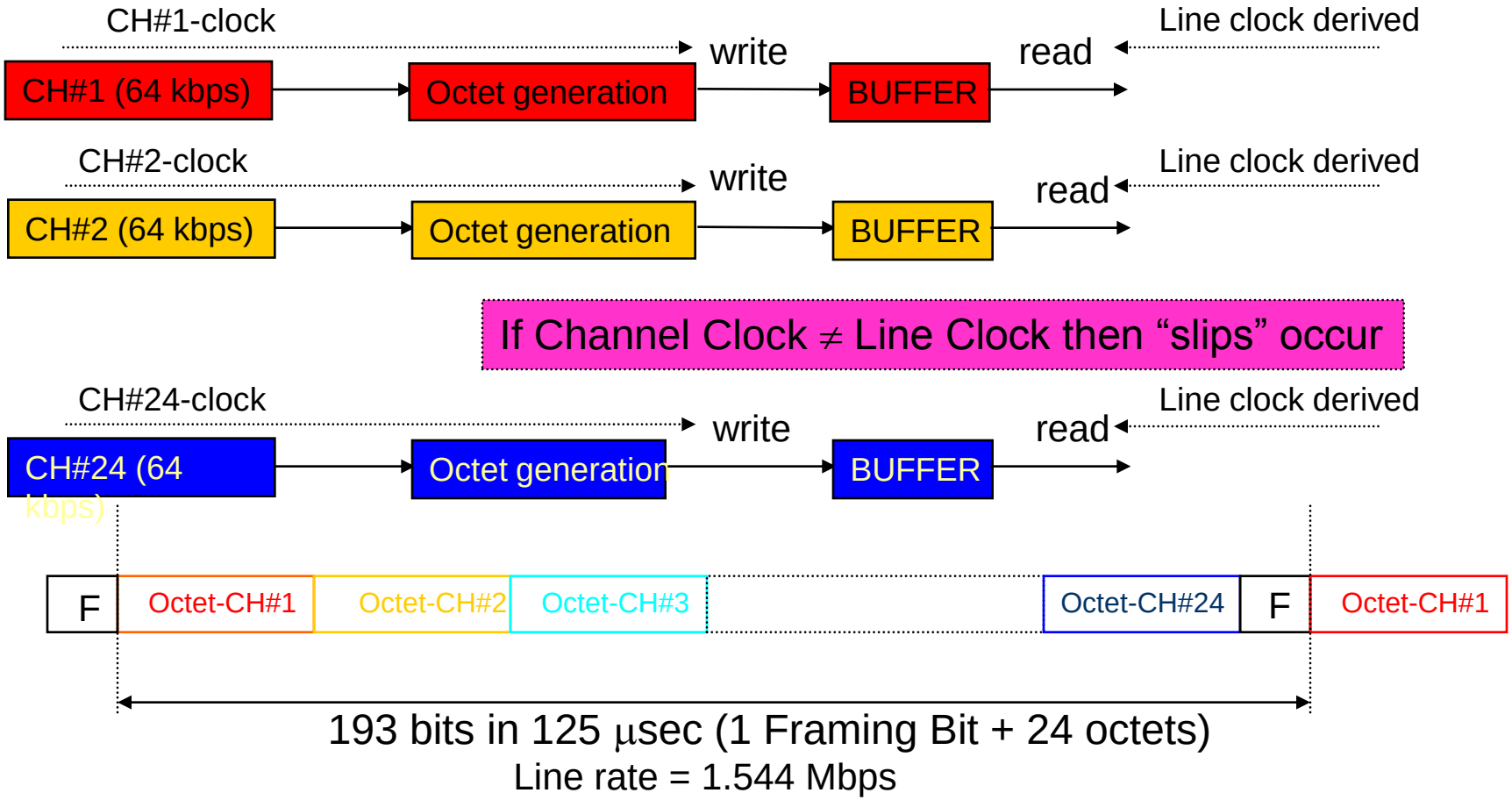


- Mobile in motion (X m/s) introduces a Doppler shift (X/c)
- When hand-over occurs, the mobile must reacquire carrier frequency
  - Loop bandwidth wide enough to handle (Δf + X/c +LO) (LO = local oscillator offset)
  - Loop bandwidth should be small from a noise rejection viewpoint
- Large Δf compromises the reliability of hand-over
- TDD networks require time/phase alignment between A & B

Timing in TDM Networks

- Synchronization is essential for synchronous multiplexing
  - To avoid information loss
- Synchronous multiplexing assemblies are used as carriers of timing information (DS1/E1, SONET/SDH)
  - The recovered clock is used as a reference for the BITS
  - The transmit signals must meet the “sync” mask for timing information
- Asynchronous multiplexing can preserve timing (up to a point) *if done correctly*
- Bearer signals (DS1/E1) in asynchronously multiplexed assemblies (e.g. DS1 in DS3) can be used as carriers of timing
  - Asynchronous multiplexing is done correctly
- DS1/E1 bearer signals in SONET/SDH are <u>not</u> suitable as carriers of (good) timing
  - SONET/SDH encapsulation of DS1/E1 was done in a way that protects data but not (good) timing information

Synchronous Multiplexing (DS1)



Switching machines such as DACS have multiple DS1s (input). Office clock (BITS) used to generate outputs.

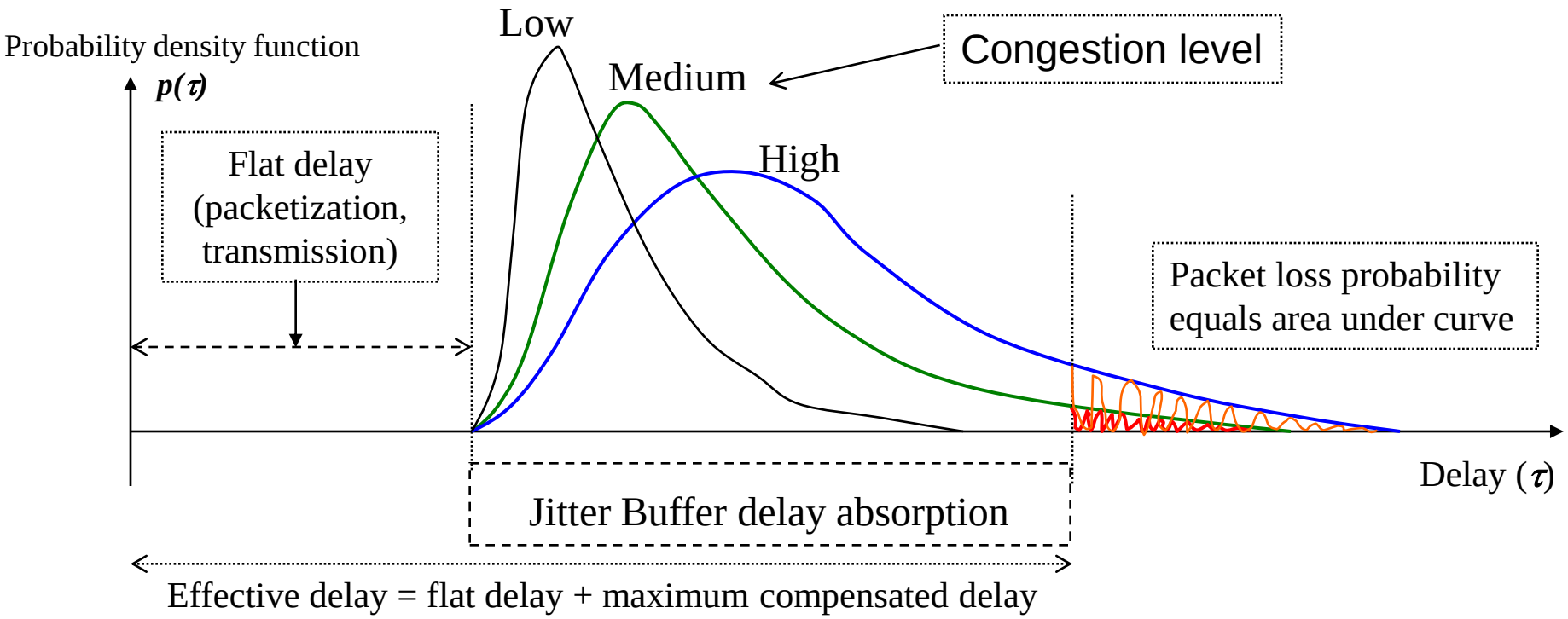
SONET/SDH : Sync and Async multiplexing

- STS-N created by interleaving N STS-1s; STM-N created by interleaving N STM-1s
  - STS-1s (STM-1s) must be synchronized (zero frequency offset between constituent channels and assembly)
  - Constituents channels of STS-1 are synchronous to STS1 (“containers”)
- Bearer channels encapsulated into “containers”.
  - e.g. VT1.5 is a container for a DS1 (1.544 Mbit/s signal)
  - The synchronizer function for DS1 → VT1.5 employs “positive-zero-negative stuffing”
- Synchronizer function differences
  - PDH uses “positive stuffing”. Clock noise introduced is high-frequency (jitter) and can be filtered out
  - SONET/SDH use “positive-zero-negative” stuffing that can introduce low-frequency (wander) components
  - DS1-bearer in PDH can be used as a synchronization reference; DS1-bearer in SONET is not used as a synchronization reference
- SONET/SDH synchronization reference carried in line clock

Timing Issues in Next Generation Networks

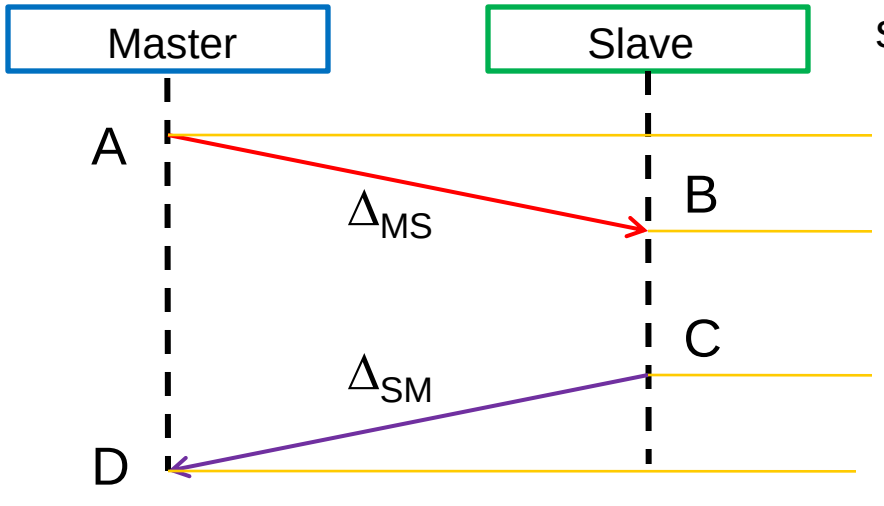
- Next generation networks are based on packet switching as opposed to circuit-switched (i.e. based on TDM)
  - Significant impact of variable delay (packet delay variation)
- Timing requirements remain.
  - Going “IP” does not mean that real-time services no longer need synchronization!
- Transition Phase:
  - Hybrid Networks (IP/TDM islands)
  - Circuit Emulation
- Timing over Packet Networks (packet-based methods)
  - PTP, NTP, adaptive clock recovery
- Monitoring and Testing
  - Metrics for packet-based timing methods (quantifying PDV)

Impact of Packet Delay Variation – VoIP example



- Jitter buffer size: trade-off between latency and packet loss
  - Minimize latency (delay) for voice calls
  - Minimize packet loss for data (voice-band modem) calls
- "Adaptive" jitter buffer techniques adjust buffer size to match time-delay-variation
  - Introduce delay for "faster" packets
  - Frequency offset (wander) is a problem

Principles of Packet-based timing methods



$$\varepsilon = \left(\frac{1}{2}\right)\left(t_4 - \tau_3 - \tau_2 + t_1\right)$$

$$\Delta_{MS} = \Delta_{SM} = \left(\frac{1}{2}\right)\left(t_4 - \tau_3 + \tau_2 - t_1\right)$$

- One exchange of packets (M-to-S and S-to-M) provides 4 time-stamps
  - Master knows t_1 and t_4 ; Slave knows τ_2 and τ_3
- t_x is correct time (master) ; τ_x is the slave's idea of time (offset of ε)
- Assumption: transit time from master-to-slave (Δ_{MS}) is equal to the transit time from slave-to-master (Δ_{SM})
- "Errors" arise because the transit time is not the same from packet to packet (packet delay variation) and the path is not reciprocal ($\Delta_{SM} \neq \Delta_{MS}$)

PTP and NTP

- Similar in principle, differences in details
  - Both use 4 time-stamps (basic two-way-time-transfer principle is common to both)
- Standards:
  - NTP: developed by IETF (RFC 5905) (now V4)
  - PTP: developed by IEEE : IEEE-1588-V2 geared to telecom req.
- Origins:
  - NTP developed to provide time-of-day to PCs, workstations, etc., over the big bad Internet
  - PTP developed to provide alignment of robots on a manufacturing floor
- Source and Sink:
  - PTP: each “slave” has one “master” (one *master* per community)
  - NTP: each “client” can query multiple “servers” and do some fancy averaging (the “community” is not well defined)

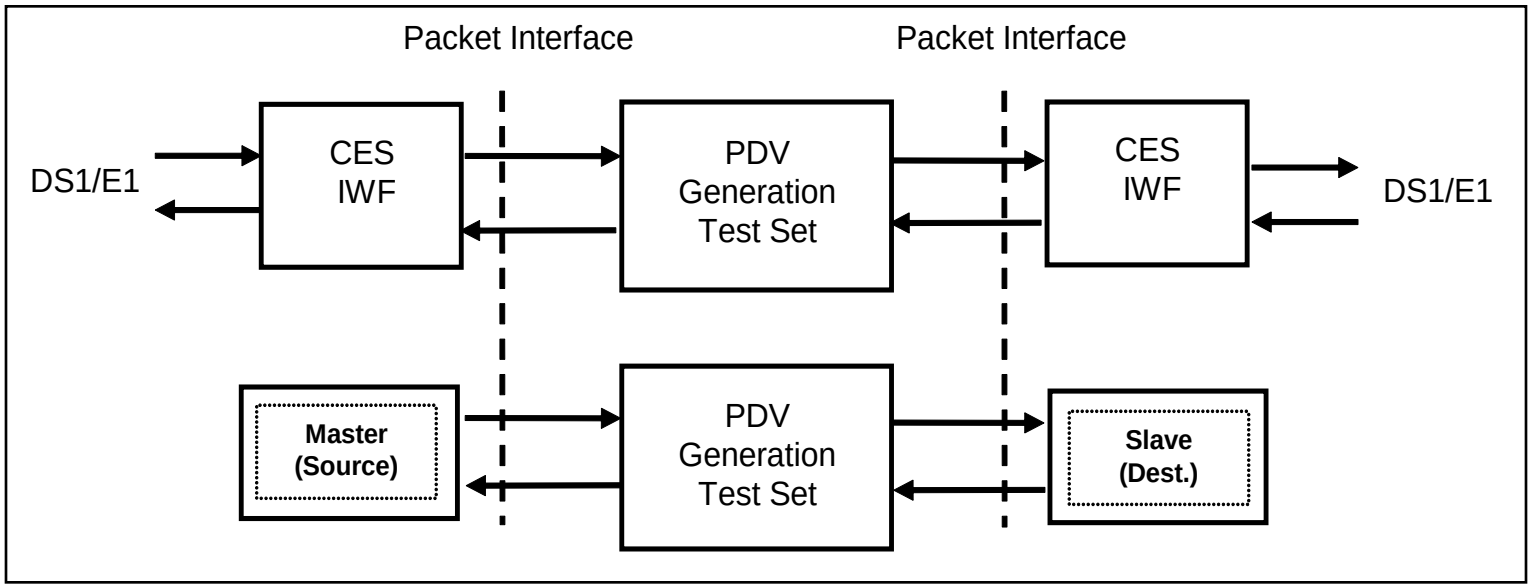
PDV Metrics

- Metrics that quantify PDV and share light on the ability of slave clocks to properly recover timing (phase and/or frequency)
- General background principles:
  - Not every packet has “good” timing information. Excess PDV is best ignored (“packet selection”).
  - For a given path, the floor delay is not load dependent though large PDV may make it “unobservable”.
  - Metrics often characterize the “floor behavior”, quantifying:
    - Amplitude distribution (pdf) of the PDV to indicate the number of packets that are near the floor
    - the temporal/spectral characteristics of the PDV associated with these packets (xTDEV)

Testing Packet-based Timing

- Packet networks are inherently hostile to timing transfer
  - Packet loss
  - Packet delay variation
  - Asymmetry
- Testing Issues:
  - No two routers are “equivalent”
  - Load behavior is statistical
  - Repeatability of tests
- Repeatable Approach:
  - Simulate/emulate a network with well-defined anomalies
- Given a particular signal processing scheme (compression, PLC, etc.), the network can only degrade QoE (never improve it). The key network properties are:
  - Packet loss profile (error rate, distribution, etc.) (and excess PDV)
  - Packet delay variation (timing)

Why Network Emulation?



- Alternative set-up for assessing performance of CES IWF or timing_over_packet
- Requires PDV Generation Test Set
- PDV Generation Test Set adds *pre-computed* delay to each packet
- Eliminates uncertainty of switch pedigree
- Permits “repeatable” testing and independent verification
- Suitable for standardization purposes

Concluding Remarks

- Timing Alignment is Fundamental in Telecommunications
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- Timing in Next Generation Networks
  - Impact of packet delay variation (PDV)
  - Testing packet-based timing transfer methods
- Backup Slides available

Questions?

Thank You for Listening

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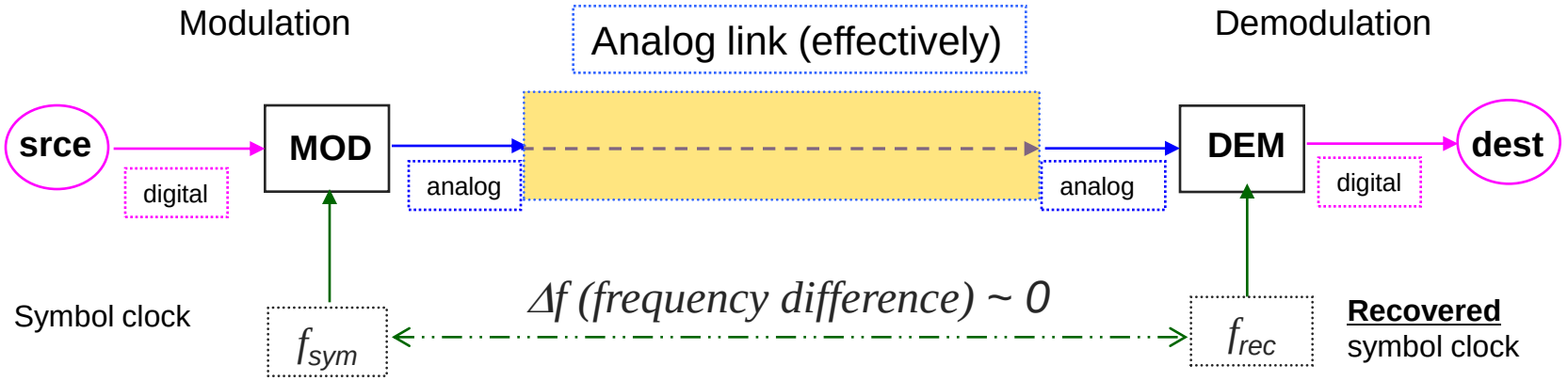
Backup Slides Follow

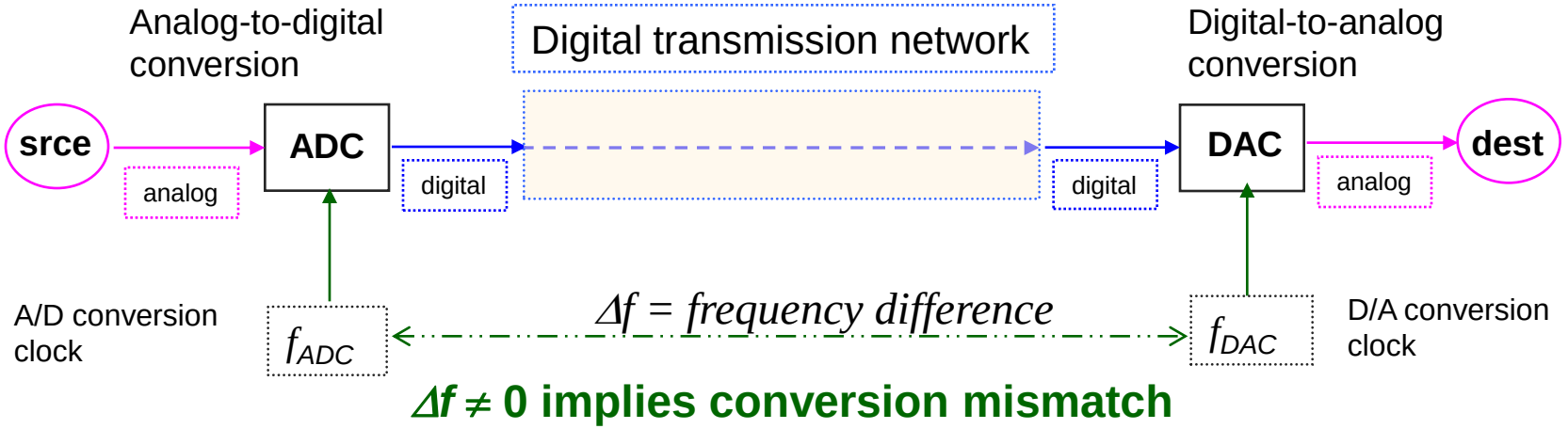
BACKUP SLIDES

Binary data transmission schemes use modems



- Source/Destination : modulator and demodulator
- Transmitter (modulator) uses a particular symbol clock
  - receiver (demodulator) must extract this clock ($\Delta f \sim 0$) for proper data recovery
- The “Analog link” must, *effectively*, mimic an analog wire pair
  - Frequency translation (e.g. DSB-AM) is benign, Doppler (pitch modification effect, PME) is not benign ($\Delta f \sim$ Doppler)

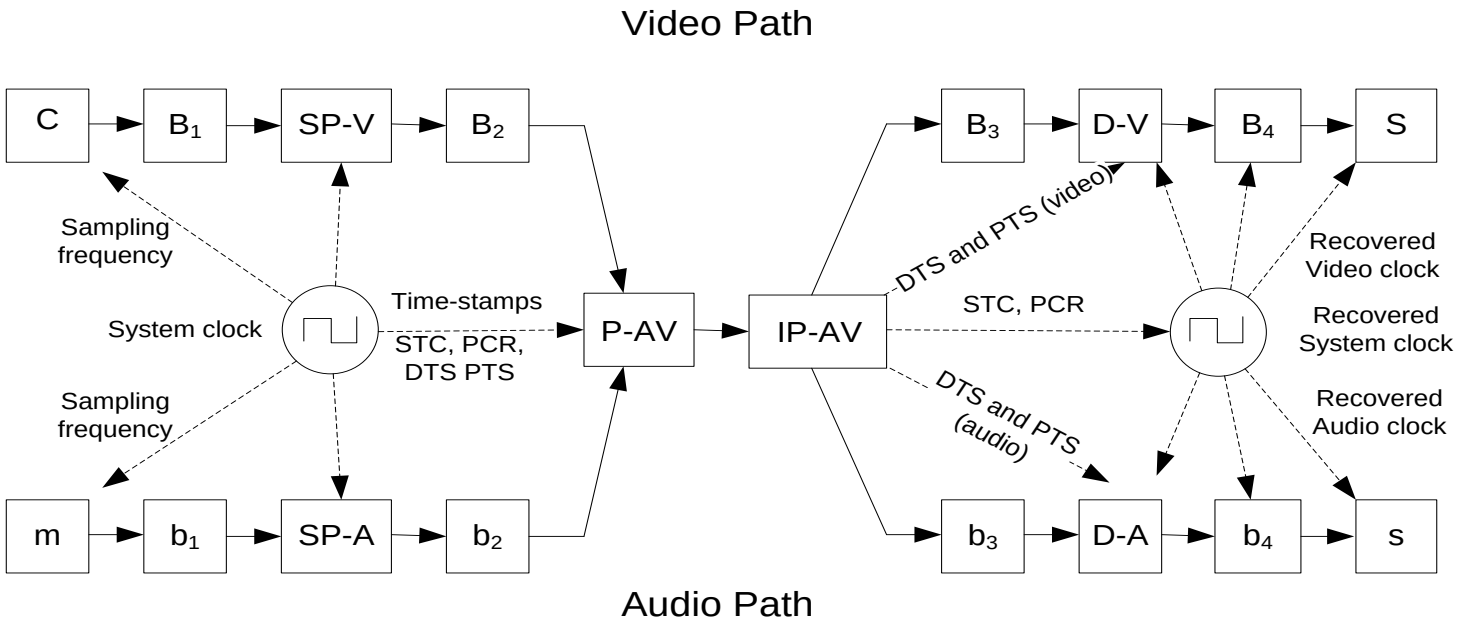
Timing Alignment in Voice-Band Transmission



Primarily affects voice-band data (Fax, modem) and real-time video

- Source/Destination : Voice/video/fax terminal
- The digital transmission network *emulates* an analog circuit (the original circuit emulation)
- Impact of frequency difference (Δf):
  - Eventually buffers will overflow/underflow (e.g. slips) (“obvious”)
  - Pitch Modification Effect (PME) (analogous to *Doppler*) makes recovered symbol clock ≠ transmit symbol clock (not so “obvious”)
  - Recovered waveform ≠ original waveform (more than just additive noise)

Timing Alignment in Multimedia

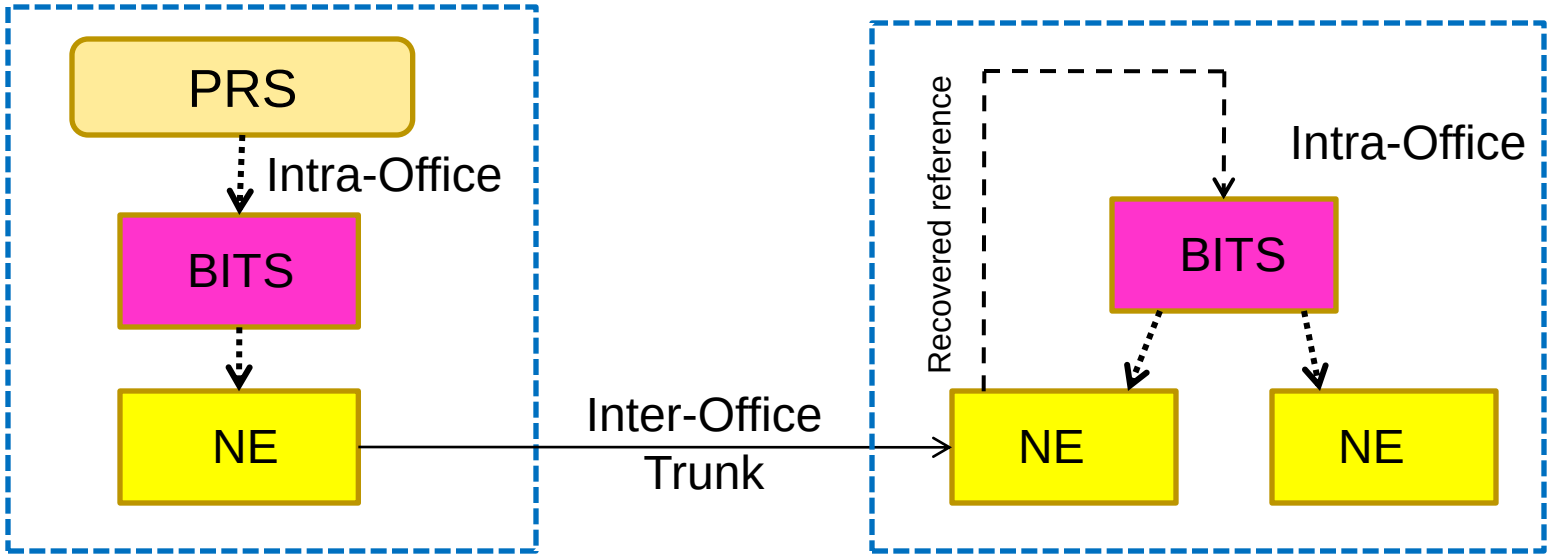


- Frequency offset (wander) between audio and video sampling results in loss of lip-sync
- Frequency offset (wander) between send-side and receive-side system clock results in freeze (video), breaks (audio), and possible loss of lip-sync

The Synchronization Network

- Synchronization distribution is best visualized as an overlay network
  - Traffic carrying transmission medium can carry a timing reference (DS1, SONET/SDH, SyncE)
- Each “node” (Central Office) has a main clock system (BITS or TSG) that provides timing to all the NEs in the office
  - The transmit out of all NEs is timed (effectively) by this signal
  - Must meet a tight mask (“sync” mask) for output signal
- Recovered clock from (usually two) incoming trunks is provided as a reference to the BITS
  - The BITS has a stratum level (ST2E, ST2, ST3E)
    - Defines the holdover performance
  - Narrow-bandwidth filtering (bandwidth <~mHz) removes significant amount of wander
- SSM (Synchronization Status Messaging) used to identify the trail and avoid *evil timing loops*

Timing distribution : PRC/PRS, BITS, NE



- PRS: *Primary Reference Source* – provides stratum-1 quality output signal
  - Cesium Atomic Reference or GPS-receiver with high-quality oscillator (Rb or OCXO)
  - Aka PRC or *Primary Reference Clock* (ITU-T terminology)
- BITS: Building Integrated Timing Supply (also TSG – Timing Sig. Gen.)
  - Provides clock reference to the different NEs in the CO (DS1/E1 most common formats)
  - Accepts a reference input and performs clock-noise filtering (removes jitter/wander)
  - Provides HOLDOVER in case of reference failure
- NE: Network Element (e.g. SONET) – uses BITS timing for its outputs
  - Recovers clock from incoming signal and provides a reference for the BITS (DS1/E1 format)

Synchronization in TDM Networks – Key Points

- Delivery of information can be compromised by absence of synchronization
  - Especially true for “analog” and CBR signals
- Synchronous multiplexing requires that bearer channels and assembly be synchronized
  - Rate adaptation in DS1/E1 achieved by slip buffers; $\Delta f \neq 0$ leads to data corruption
  - SONET/SDH also use synchronous multiplexing to get the higher bit-rates
- Asynchronous multiplexing requires that the bearer channel be rate-adapted (bit stuffing) to channel rate
  - Positive stuffing introduces high-frequency noise (jitter) (PDH)
  - Positive-zero-negative stuffing introduces wander (SDH)
  - Bearer channel clock noise is sum of stuffing noise (filtered) and assembly clock noise
- SONET/SDH bearer signals not suitable as synchronization reference
  - Derived DS1/E1 based on optical line-clock used as a synchronization reference

Timing Considerations — TDM

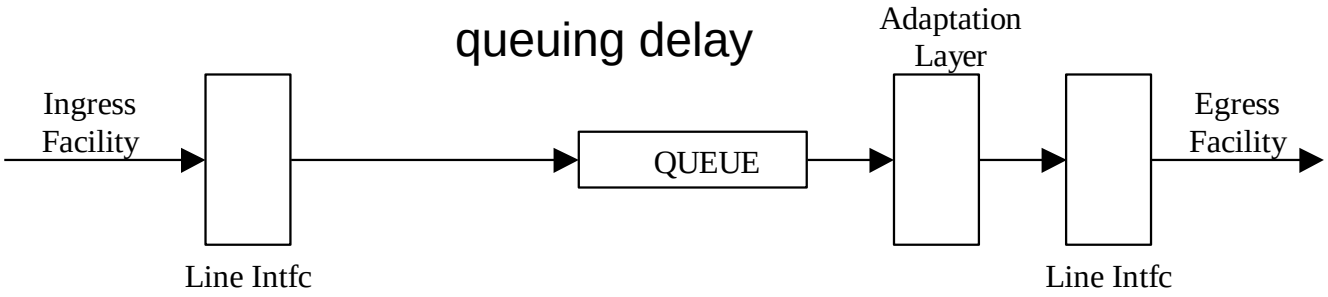
- Supporting real-time services require timing (frequency) at the conversion points (e.g. A/D and D/A converters) (regardless of transport mechanisms)
  - Future requirements may include both frequency and time ("Time-of-Day")
- Circuit Switched Network ("TDM") requires timing (frequency) in order to maintain transport data integrity
  - Transmitted signal is "continuous"
    - Frequency offsets "absorbed" by slip buffers (not error free)
  - Recovered clock from physical layer can be a timing reference
  - Delivery of timing reference to the end-points is straightforward
    - e.g. DS1 IADs can use loop-timing, deriving timing from the network by using the DS1 recovered clock as a reference**
  - *Synchronizing the transport network indirectly provides the timing required to support real-time services*

**: Very Important

Timing Considerations — Packet

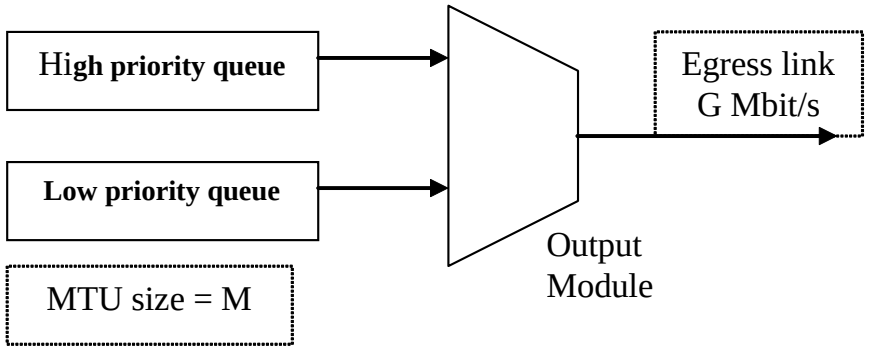
- Real-time services require timing (frequency) at conversion points (e.g. A/D and D/A converters; C-to-P conversion points) (regardless of transport mechanisms)
  - Future requirements may include both frequency and time ("time of day")
- Packet Networks may not require timing (frequency) to maintain transport data integrity…..
  - Data transfer is bursty, with "gaps" and time-delay variation
    - Frequency offset "absorbed" by jitter buffers; errors caused by overflow/underflow
    - Buffers can be made large (with a latency penalty)
  - Delivery of sync reference to the end-points, for supporting real-time services, is still required and just may be "natural" as in TDM
    - How does an IAD fed by Ethernet get its synch. reference? (SyncE!)
  - *Common misconception that since transport does not require it, timing is "not necessary" (overlooking requirement of service)*

Packet Delay Variation — Primary Causes



All routers have queues to handle QoS (priority mechanisms)

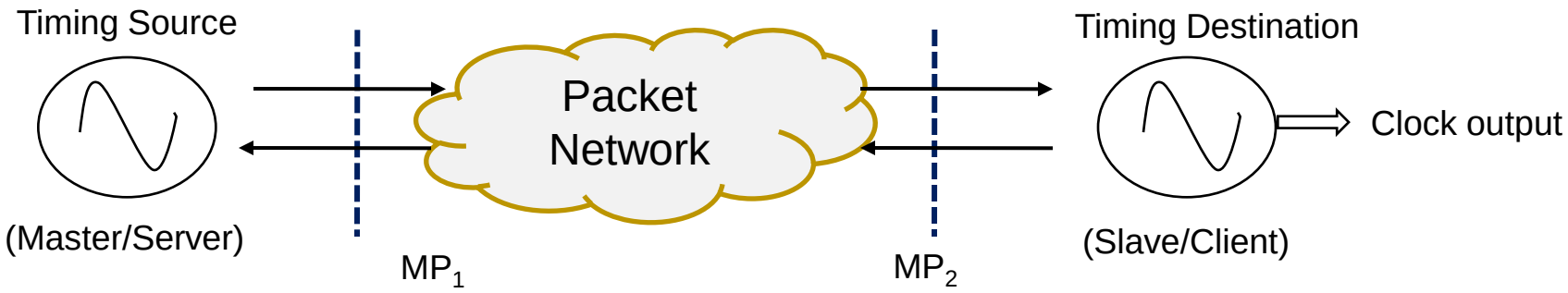
Head-of-line blocking



Even the highest priority traffic can be held up at the output buffer.

$$\left(\Delta_{pp}\right)_{\max} \geq \left(\frac{M}{G}\right) \mu s$$

Packet Delay Variation – definition (Y.1540)



- IP Packet Transfer Delay (IPTD): $x_k = t_2(k) - t_1(k)$
  - $t_m(k)$ = time that packet "k" traverses MP
- Reference delay: $d_{1,2}$ (something "fixed"):
  - x_0 (first packet)
  - *average over "recent" past*
  - *minimum over "recent" past*
  - other (affects just the mean value, not variance or spectrum)

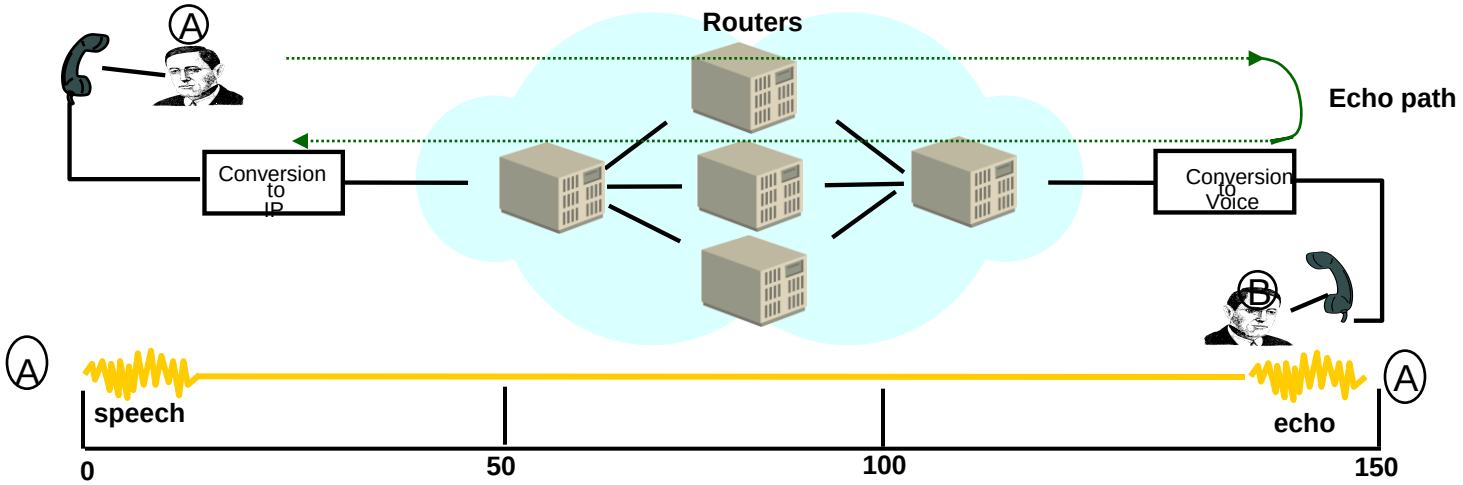
Commonly used for sync discussions

- 2-point IP Packet Delay Variation : $v_k = x_k - d_{1,2}$
- 1-point PDV(at MP_2) : $y_k = t_2(k) - T_2(k)$
  - $T_2(k)$ = expected time of arrival of k^{th} packet, e.g. based on periodicity
  - $T_2(k)$ = time-stamp in k^{th} packet (essentially ignoring $d_{1,2}$)
  - Well-suited for CES and other packet-based (frequency) methods

Impact of PDV – VoIP example (contd.)

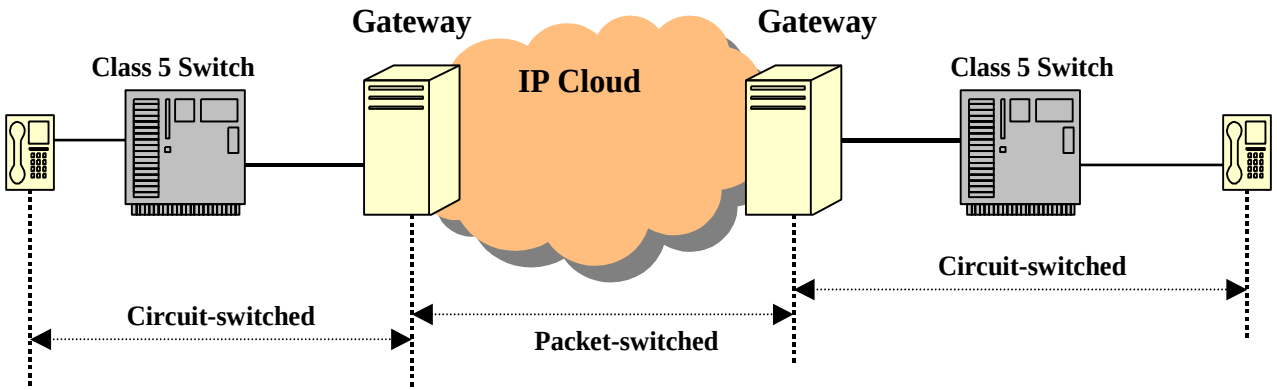
Latency can degrade the quality of experience.

For acceptable QoE, *echo return loss* (ERL) requirement increases with delay.



- With 40 dB ERL, R-rating drops 20 points as one-way delay increases from 0 to 150 msec.
- With one-way delay > 100 msec, R-rating drops 50 points if ERL drops from 40 dB to 20 dB.
- QoE drops rapidly if one-way delay increases beyond 150 msec.
- Jitter buffer is a major contributor to delay – PDV increases size of JB

Timing implications – VoIP example (contd)



Scenario: IP segment replaces TDM segment

- Increase in latency implies Echo Canceller (EC) required in Gateway.
- Class 5 ERL ≈ 15 dB implies EC ERLE required ≈ 25 dB.
- *Entire circuit-switched segment in tail circuit of EC.*
- *Any slip in circuit-switched segment introduces a tail-circuit nonlinearity.*
- *Non-linearity episode introduces a "blip", reducing EC ERLE momentarily.*
- *Slips thus introduce a decrease in QoE.*

Conclusion: Replacing TDM segment with IP may require a tightening of timing (holdover) requirement in (remaining) circuit-switched segment.

Circuit Emulation

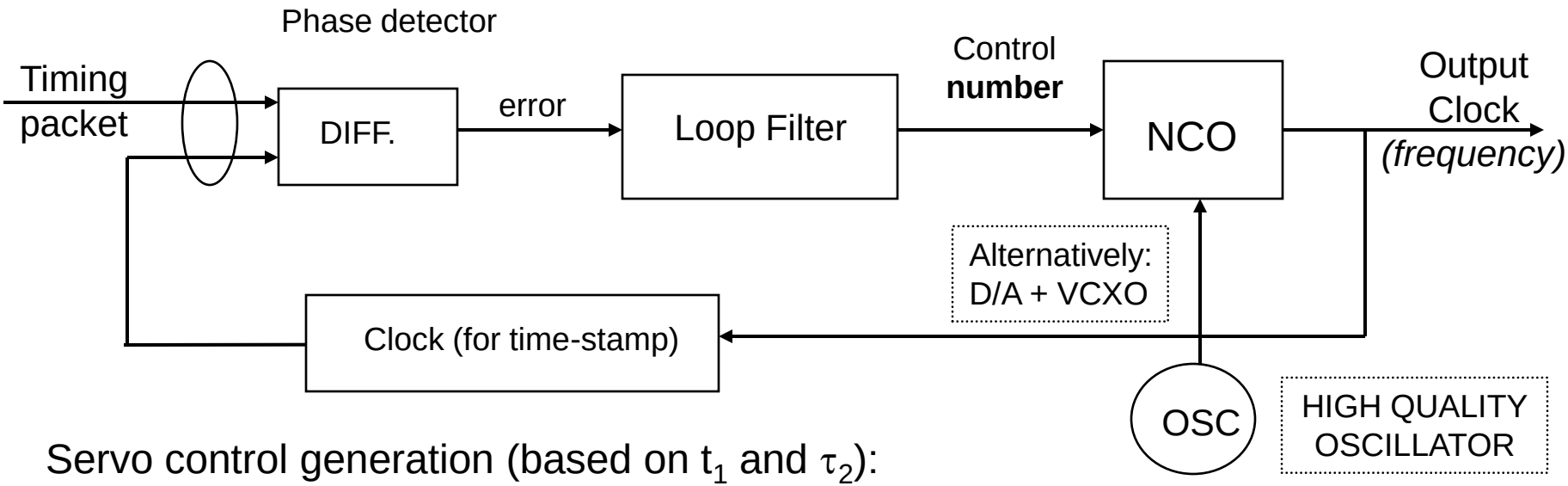
- Principles of Circuit Emulation. *What is it*?
  - Circuit Emulation refers to packet-based techniques that "mimic" circuit-switched implementations. This implies:
    - Bit integrity. No loss of "information".
    - Bit-time integrity. Meeting specifications of frequency transfer, jitter, and wander.
    - Meeting "legacy" specifications at the interface points.
    - Keeping transmission delay (latency) as low as possible.
      - This is often overlooked!
- Summary of clock recovery approaches given in ITU-T Rec. G.8261
  - Network Synchronous ("retimer")
  - Differential Methods
  - Adaptive Methods
  - Loop Timing (The "null" case)

Network synchronous and differential methods require a "network clock" reference. Best obtained by PTP/NTP (or physical layer)

PTP and NTP – some distinctions

- Different notion of “Time 0”
- Different formats for time-stamps
  - PTP limit : 2^{-32} s (tenths of nanoseconds)
  - NTP limit : picoseconds
- Initiator:
  - NTP: client initiates interaction. Request to Server who replies.
    - S-M Query; M-S Response
  - PTP: Master speaks (twice!), Slave listens and occasionally asks a question and Master responds.
    - M-S Sync and Follow-up; S-M delay-request and M-S delay-response
- PTP has the notion of *on-path support – aka transparent clocks*
- PTP community of clocks may have to decide who is Master (*aka Best Master Algorithm*)
- Different (artificial) limits on packet rate

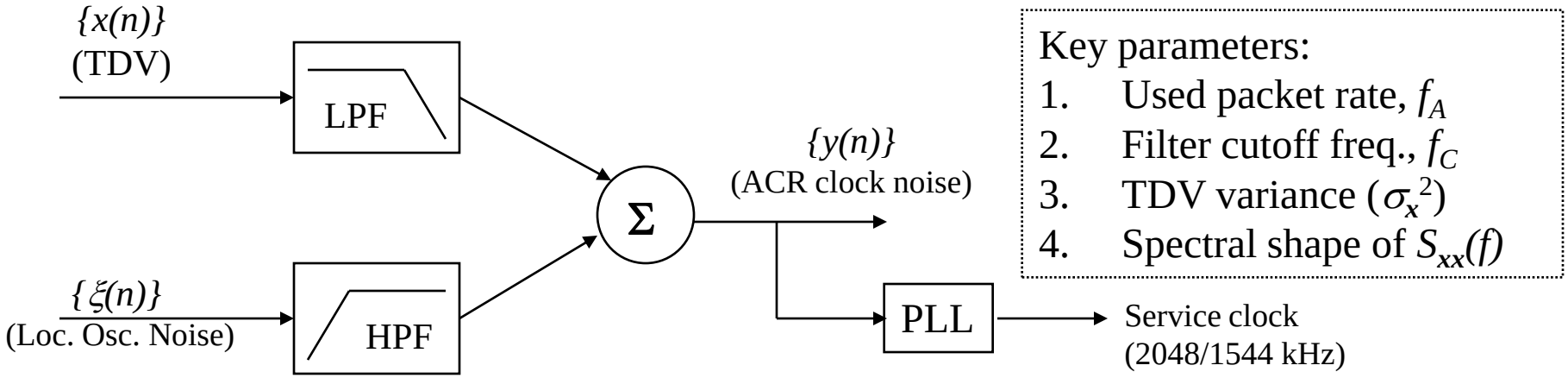
Timing over packet – frequency (one-way)



Servo control generation (based on t_1 and τ_2):

1. Time-stamp for time-of-arrival based on local clock
2. Time-stamp for time-of-departure based on master (source) clock and is present in the packet or follow-up or implied
3. Difference in time-stamps should (ideally) be a constant (this concept used for servo control)
    1. Local clock error (frequency offset) contributes to difference (we are trying to correct this)
    2. Variation in transit delay (packet delay variation) contributes to difference (this is extraneous noise and deleterious)
4. Alternatively use other direction (based on t_4 and τ_3)

Timing over packet – frequency (one-way)



- Clock Recovery utilizes a phase/frequency locked loop to smooth out (low-pass filter) the time-delay-variation in used packet rate (f_A)
  - Commonly referred to as *Adaptive Clock Recovery*
  - Second PLL used to generate the actual service clock rate (e.g. 1544kHz)
- Recovered clock noise variance (wander) directly proportional to TDV variance (as seen by the phase locked loop!)
- Most benign case: time delay variation has a flat spectrum (“white phase noise”)
- The loop appears as:
  - low-pass filter to the “reference clock noise” (time-delay variation associated with the used packets) [impacts wander]
  - high-pass filter to clock noise associated with the local oscillator [impacts jitter]

General requirements for packet-based metrics

- The basic parameter is the packet delay variation (PDV)
  - Equivalent to “time error”
  - ITU-T Rec. Y.1540 provides definitions for packet delay variation
- Some processing of the PDV data is needed to get a proper interpretation of the packet network behaviour (metrics)
- Different metrics may be defined and these may have some relationship with hypothetical clock-recovery algorithms (e.g. packet selection)
- Traditional IP network metric (i.e. peak-to-peak jitter) is generally inadequate
- Metrics considered and still under consideration:
  - MTIE, TDEV (traditional clock metrics still in use)
  - minTDEV, clusterTDEV, percentileTDEV, bandTDEV (other members of the TDEV family) (different packet selection methods)
  - MATIE, MAFE (variations of MTIE) (including averaging in MTIE)
  - Probability density function (pdf) and its Fourier transform
  - And many more to come

Why Network Emulation?

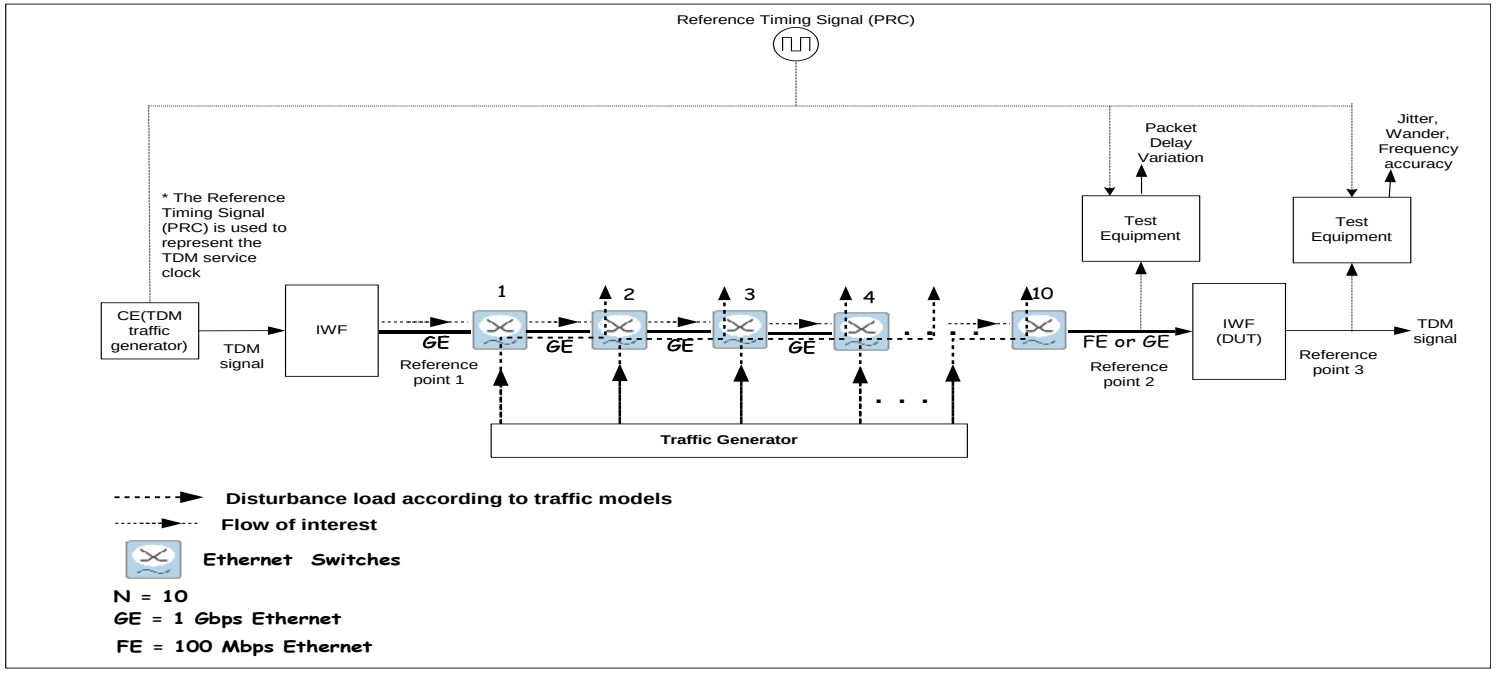


Fig. VI.4/G.8261 – Performance Test Topology (G.8261)

- Typical set-up for assessing performance of CES IWF (from G.8261)
- Requires several units (switches, traffic generators, etc.)
  - May be affected by choice of switch (model/manufacturer)
  - May be affected by manner in which traffic generated for loading
  - May be affected by …..

Packet Network Testing – a rational approach

- Next generation test sets will emulate networks in terms of PDV (and packet loss profiles if necessary)
- Pre-determined PDV profiles will allow repeatable and “deterministic” test results
- Eliminates dependencies on manufacturer specific aspects of packet-switching network elements an method of introducing interfering traffic
- Suitably chosen PDV profiles will permit standardization of performance requirements
- PDV profiles can be created via simulation models, synthetic sequences as well as actual measurements

Recap – Timing in NGN

- Going “IP” does not mean that real-time services no longer need synchronization!
  - Timing requirements based on Transport and Service
- Transition Phase – Hybrid Networks
  - Increased delay brings its own issues (e.g. echo)
  - Circuit Emulation
- Timing over Packet Networks
  - Two-way time transfer
  - PTP and NTP
- Packet Delay Variation and Metrics
- Testing Issues

Standards Bodies, Workshops, Forums

- ITU-T – International Telecommunication Union – Telecom Sector (United Nations)
- ATIS – Alliance for Telecommunications Industry Solutions
- ETSI – European Telecommunications Standards Institute
- IEEE – Institute of Electrical and Electronics Engineers
- Telcordia – Formerly BellCore
- IETF – Internet Engineering Task Force
  - TICTOC – Timing over IP Connection and Transfer of Clock
- Relevant Workshops/Forums:
  - NIST - National Institute of Standards and Technology (annual Workshop on Synch. In Telecom. Systems, WSTS is co-sponsored by Telcordia, ATIS, and IEEE)
  - ITSF - International Telecom Synchronization Forum