Timing for Optical Transmission Network (OTN) Equipment

Slobodan Milijevic

Maamoun Seido

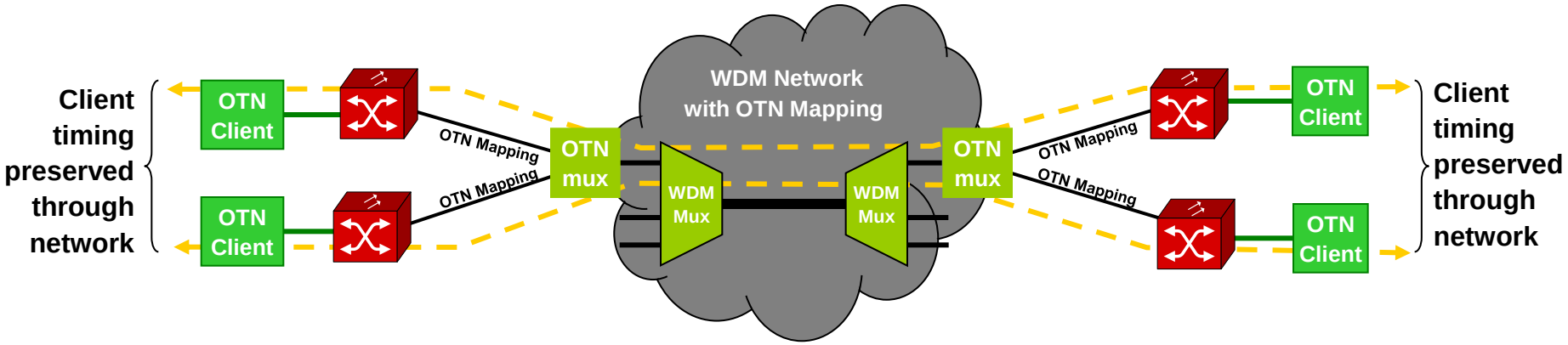
ZARLINK SEMICONDUCTOR

Agenda

- Overview of timing in OTN
- De-synchronizer (PLL) Requirements of OTN
  - Phase Gain
  - Loop Bandwidth
  - Frequency Conversion
- Overview of different De-synchronizer architectures
  - Basic PLL
  - Integer-N PLL
  - Fractional-N PLL
  - PLL with numerical feedback

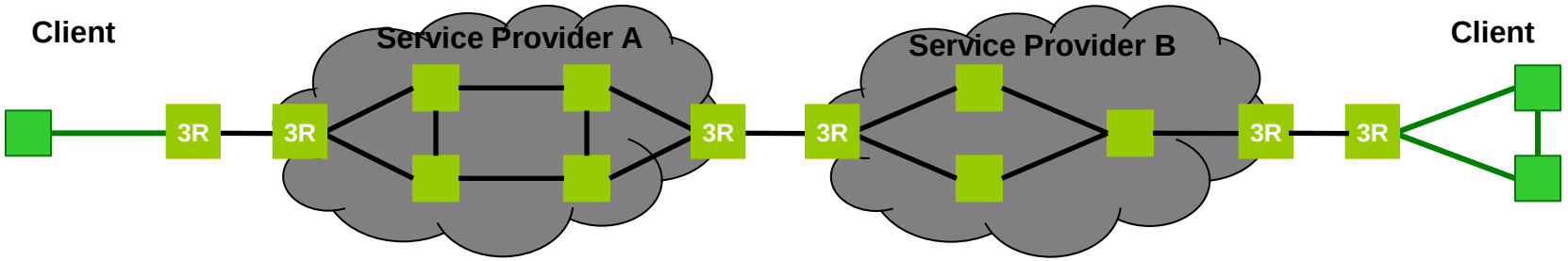
OTN Timing

- OTN physical layer is asynchronous and therefore does not require the sophisticated timing distribution associated with TDM hierarchy
  - TDM timing distribution sophistication relates to the complexity and cost to service providers for maintaining the network reference and timing hierarchy
- OTN includes per-service timing adjustments to carry:
  - Asynchronous services (GbE, ESCON)
  - Synchronous services (OC-3/12/48, STM-1/4/16, SDI)
  - Multiplexed synchronous and asynchronous services into a common wavelength



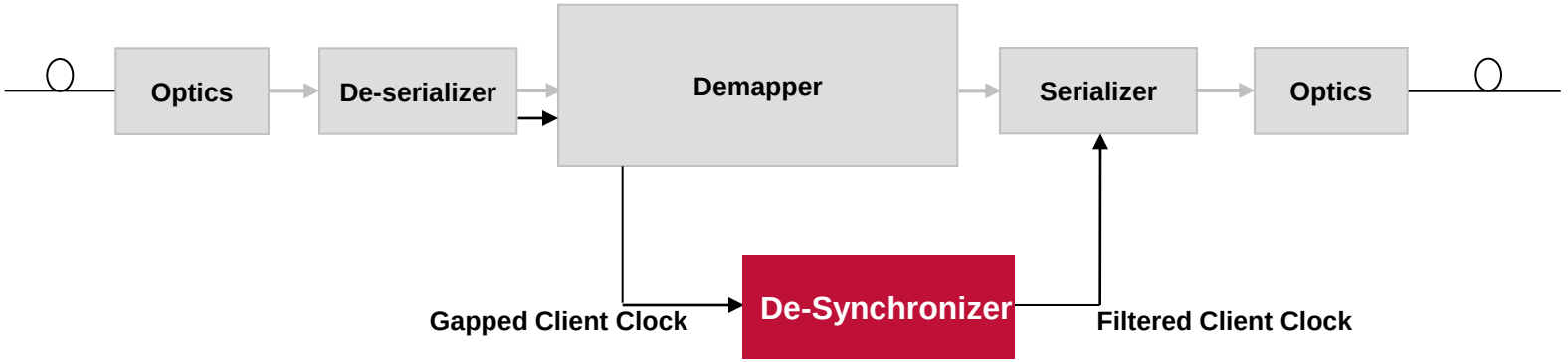
OTN Timing Transparency

- OTN's transparency enables carrying any service, including SONET/SDH, without interfering with the client timing
- Timing transparency is important for offering wholesale services for third-party providers
- Every OTN network element (Transponder, Muxponder or high order to low order mapper needs to have a de-synchronizer (PLL) with maximum BW of 300Hz
  - When carrying asynchronous clients the de-synchronizer filters jitter introduced by the de-mapping process
  - When carrying synchronous clients the de-synchronizer filters jitter introduced by the de-mapping process and embedded phase information

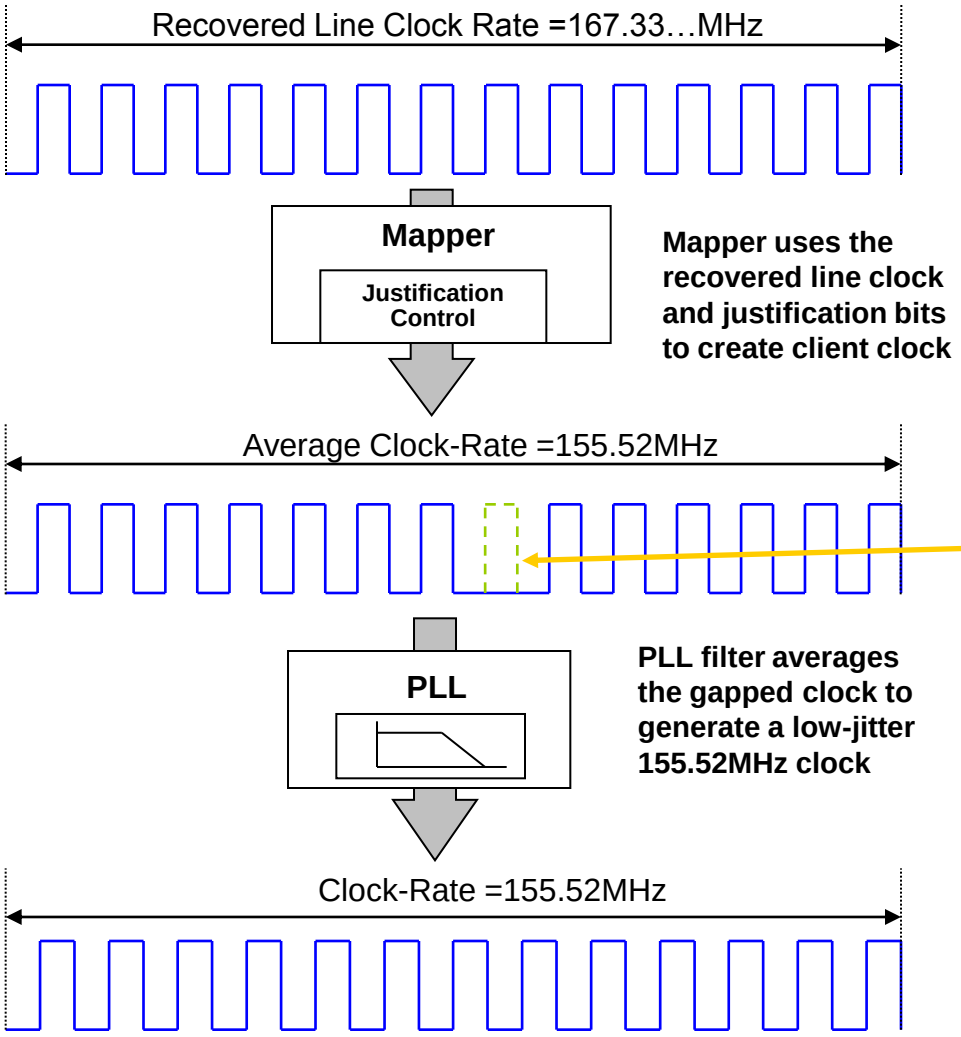


What Enables Timing Transparency!

- OTN network elements – Transponder, Muxponder or high order to low order mapper need a de-synchronizer
- The de-synchronizer is a second order PLL with a maximum 3dB cut-off (bandwidth) of 300Hz and 20 dB/decade attenuation



OTN Mapper Generated Gapped Clock



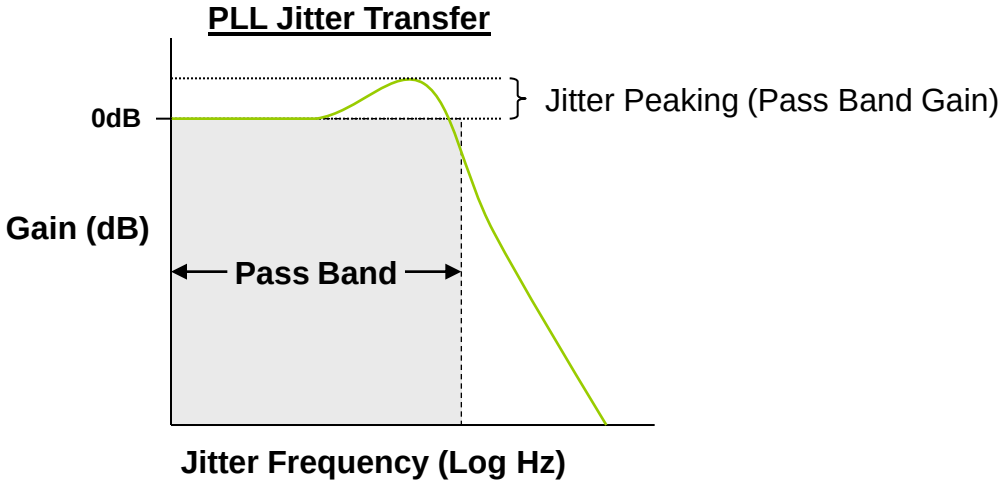
- The mapper creates the client clock rate by deleting pulses from the recovered OTN line rate. Or, the OTN line clock is “gapped” to make the average clock-rate equal the desired client clock-rate
- When the OTN carries an asynchronous client (i.e. FC), clock gaps can be added or deleted to prevent data buffer overflow or underflow conditions
- When the OTN carries a synchronous client (i.e. SDH), clock gaps can be added or deleted based on client associated phase information (justification information)

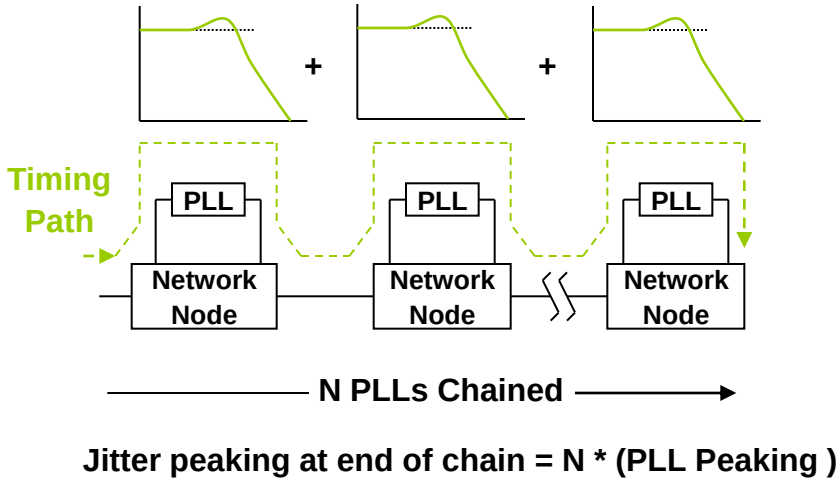
Requirements of OTN de-synchronizer

- Narrow loop bandwidth of 300 Hz
  - New G.709 has added GE clients supporting SyncE. Simulation presented at the standard shows that with the use of additional embedded phase information the 300Hz de-synchronizer BW can be used, otherwise a lower BW de-synchronizer is needed
  - During the G.709 development the addition of Video clients over OTN was introduced. Initial simulation presented during G.8251 development show that these clients will require a de-synchronizer BW in the 10Hz range (This was pushed to future revision of G.8251)
  - New G.709 has added potential more 'clients' to OTN with the introduction of ODU-Flex, each might need a different BW de-synchronizer, hence the need for a flexible loop BW
- Maximum gain peaking of 0.1dB
- Flexible frequency conversion

De-synchronizer (PLL) Gain Peaking (Pass Band Gain)

- G.8251 specs limit the jitter peaking of 0.1dB
  - Ensures accumulated jitter gain over multiple nodes does not cause timing instability

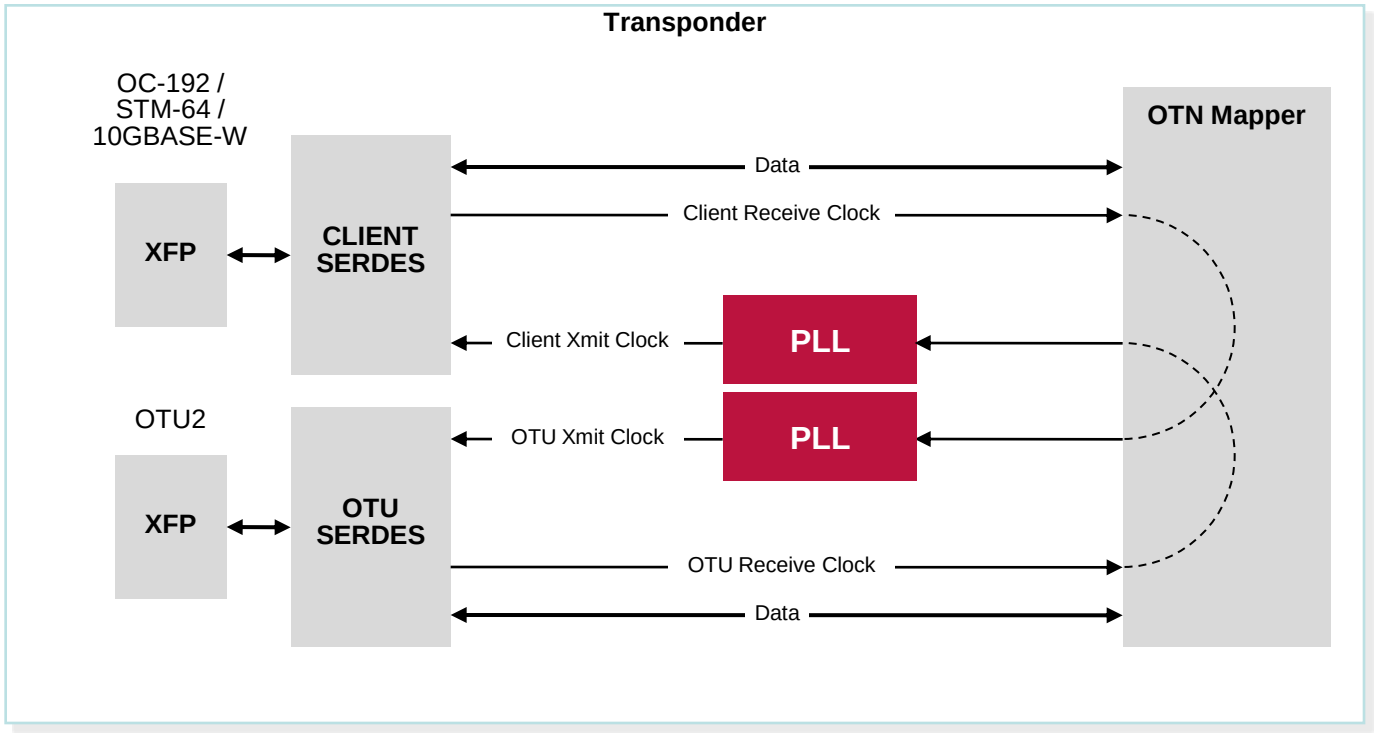




Jitter peaking at end of chain = N * (PLL Peaking)

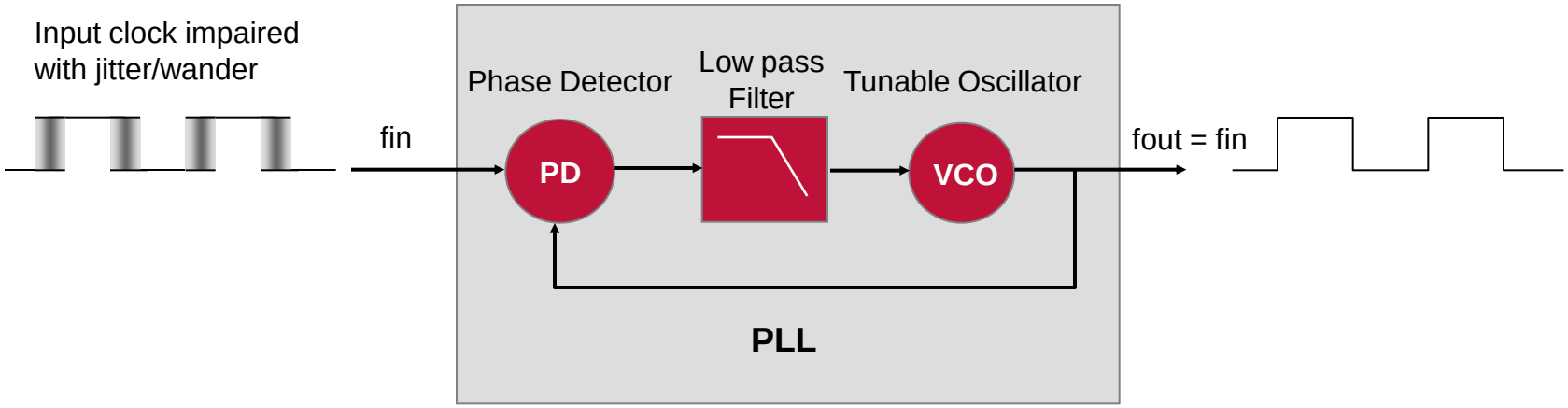
Flexible Frequency Conversion

- **Clock frequency rate translation from client side to line side rates and vice-versa**

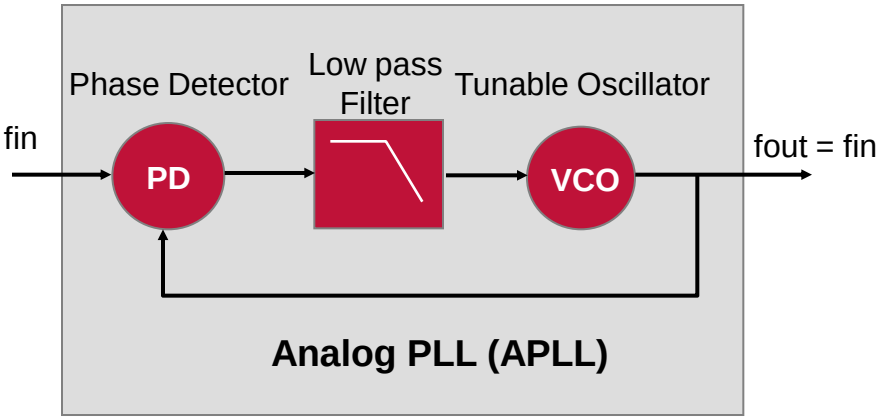


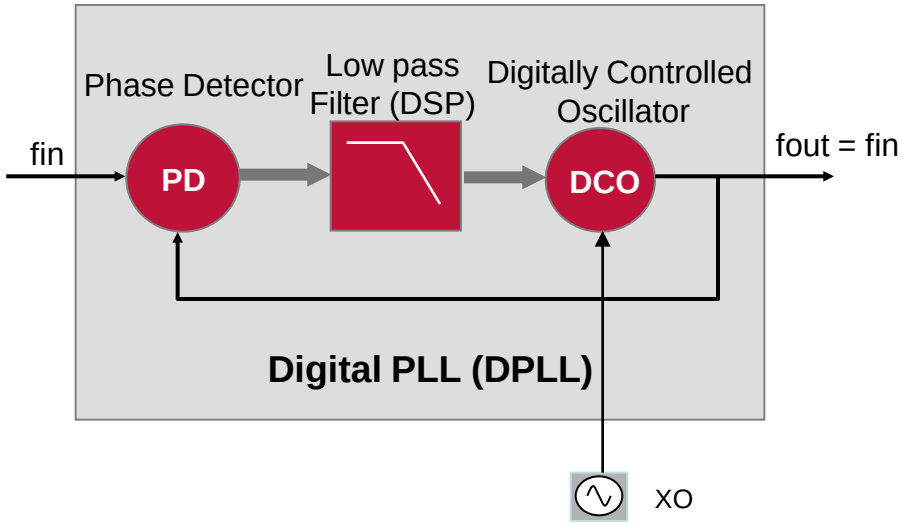
PLL- Basics

- PLL stands for Phase Locked Loop
- The PLL should be viewed as a Synchronized Oscillator
- PLL is comprised of a tunable oscillator and feedback loop. The feedback loop is used to adjust the output frequency and phase of the tunable oscillator to the frequency and phase of the input reference signal.



Types of PLLs



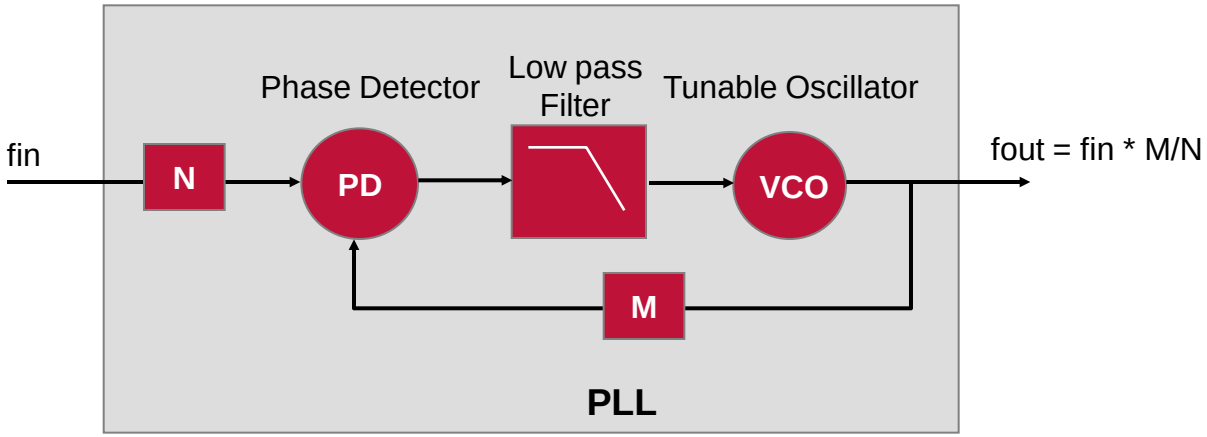


- Better at filtering jitter
- No holdover
- No hitless reference switching

- Better at filtering wander
- Very good holdover
- Provide hitless reference switching

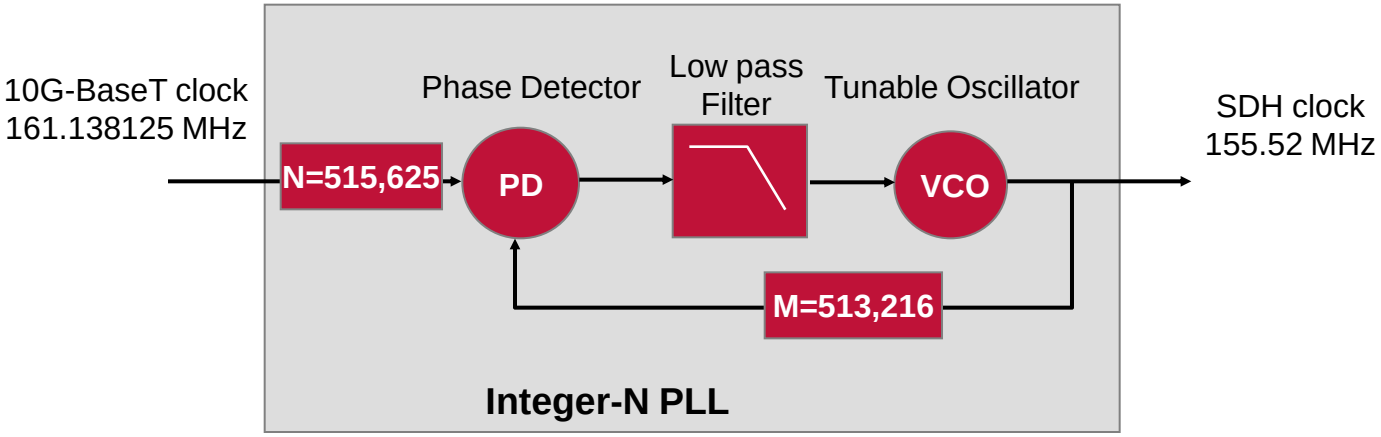
Integer-N PLL

- **Has typically two dividers: M in feedback path and N in the input path**
- **Output frequency is fout = fin * M/N**
- **Minimum frequency step is fin/N**



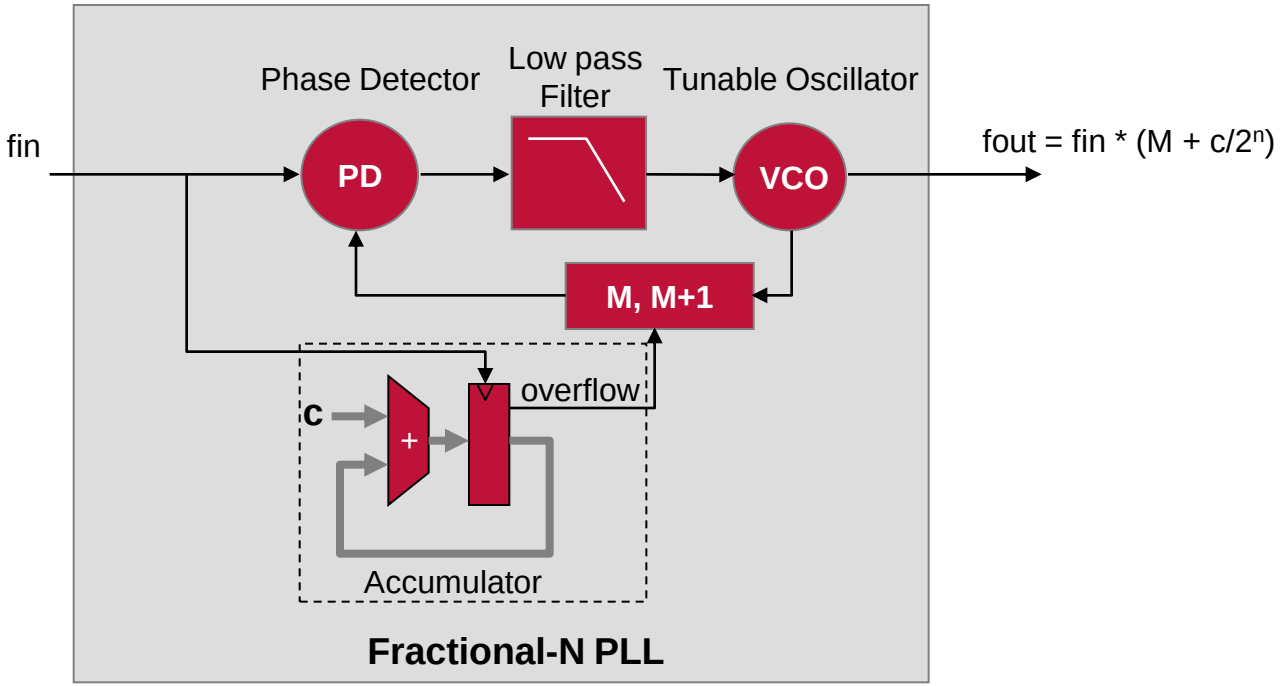
Deficiencies of Integer-N PLL

- **Minimum frequency step is very coarse (fin/N)**
- **To increase the resolution, the divider factor (N) has to be increased. This reduces the frequency of the clock fed the phase detector which in turn increases intrinsic jitter of the PLL because VCO gets very infrequent updates.**
- **Cannot have narrow loop bandwidth due to low frequency stability of their VCO which is typically implemented as a LC (L-Inductor, C-Capacitor) based oscillator in monolithic technology.**



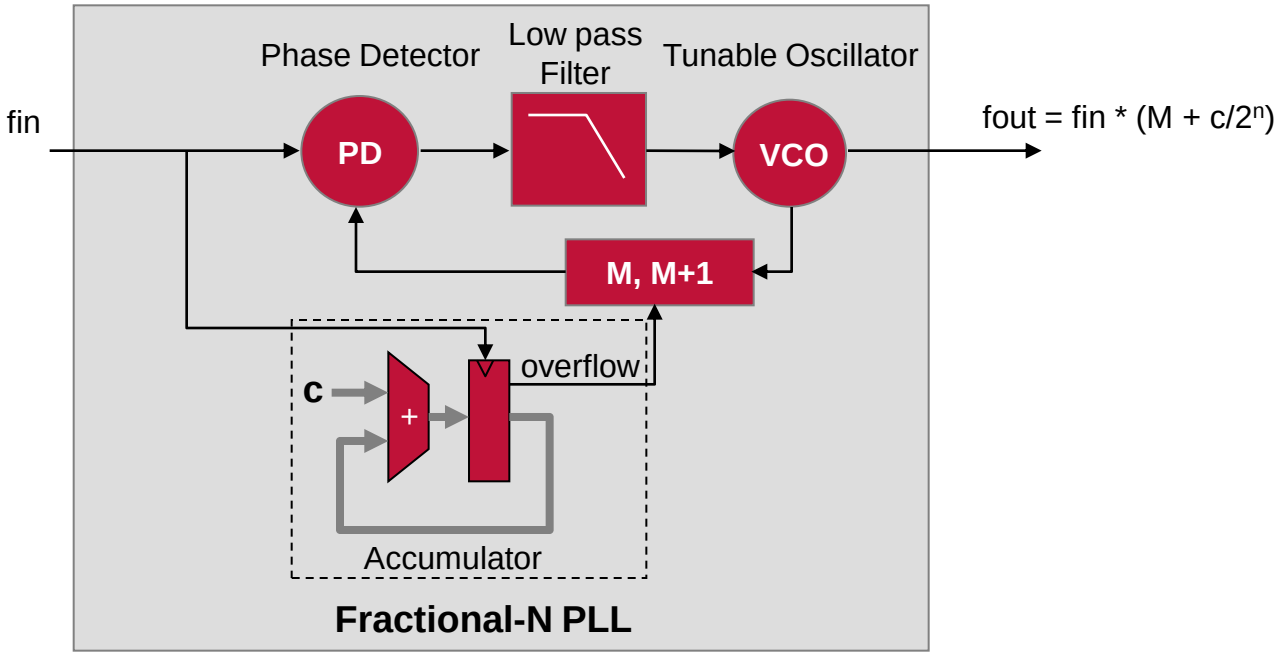
Fractional-N PLL

- **Fraq-N PLL has much higher resolution than integer N PLL because feedback divider is now fractional number.**
- **Frequency resolution is function of accumulator size (n). Minimum frequency resolution is: $fin/2^n$**



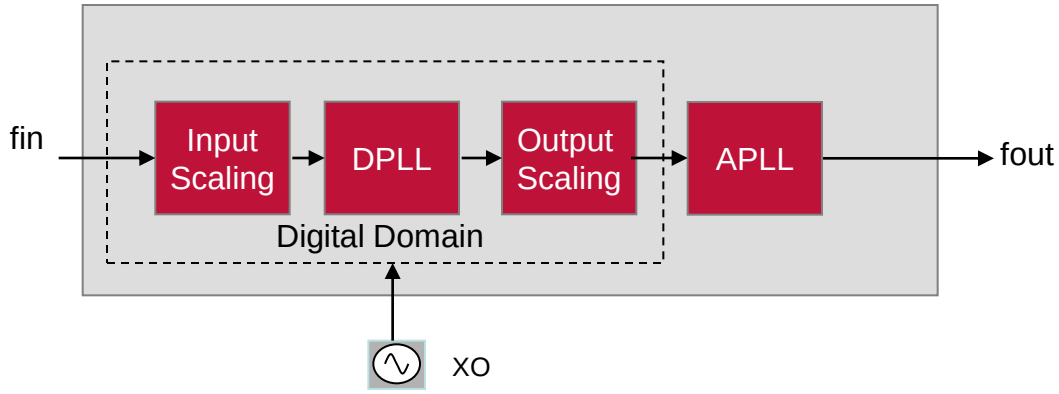
Deficiencies of Fractional-N PLL

- **Major problem are fractional spurs due to periodic changes of division ratio in feedback divider which can be mitigated up to the certain level with various techniques (phase error cancelation with DAC, Dithering, Sigma-delta noise shaping …)**
- **For fractions very close to integers, update rate of dual divider is very slow, resulting in very high low frequency spurs.**
- **Cannot have narrow loop bandwidth due to low frequency stability of their VCO which is typically implemented as a LC based oscillator in monolithic technology.**



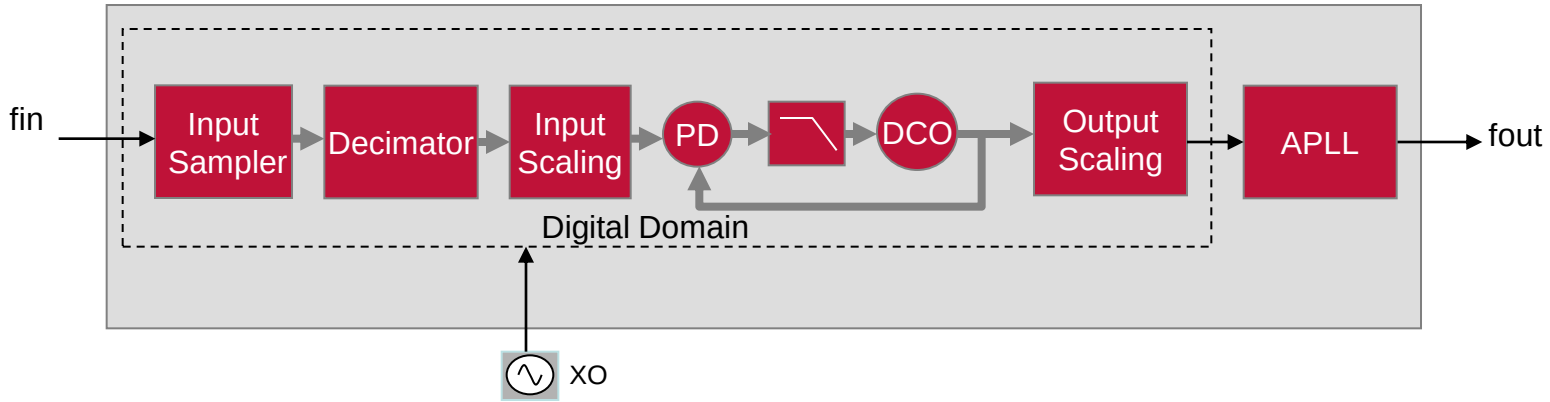
PLL with numerical feedback

- Comines advantages of both DPLL and APLL
- DPLL works at the constant rate whereas input and output frequency are independently defined
  - Input scaling circuit converts input (any frequency) to a fixed frequency excepted by DPLL
  - Output scaling circuit converts DPLL output to any frequency required by application
  - Due to its digital nature any M/N rate can be supported without performance penalties.
- APLL used just to multiply DPLL output and clean jitter.



PLL with numerical feedback Cont.

- Input sampler samples input clock at very high clock rate.
- Decimator brings down the speed of the clock to manageable by digital circuitry
- Scaling normalizes the input frequency to the frequency used by DPLL.
- DPLL provides required (programmable) loop bandwidth (less than 300Hz), holdover functionality, hitless reference switching, phase slope limiting.
- Frequency Synthesis converts normalized internal frequency to any output frequency required by the application



Thank You !