>BUSINESS MADE **SIMPLE**

Synchronous Ethernet for Next-Generation Metro Ethernet Networks

Michel Ouellette
System Architect – CTO Office
ITSF
Prague, November 14-16, 2006

NORTEL

Outline

> What is Synchronous Ethernet

> Applications of Synchronous Ethernet

> IEEE 802.3 Standards Architecture (100BASE-TX)

> Internals of a 100BASE-TX Ethernet PHY

> Experimental Setup & Results

> Summary

Synchronous Ethernet

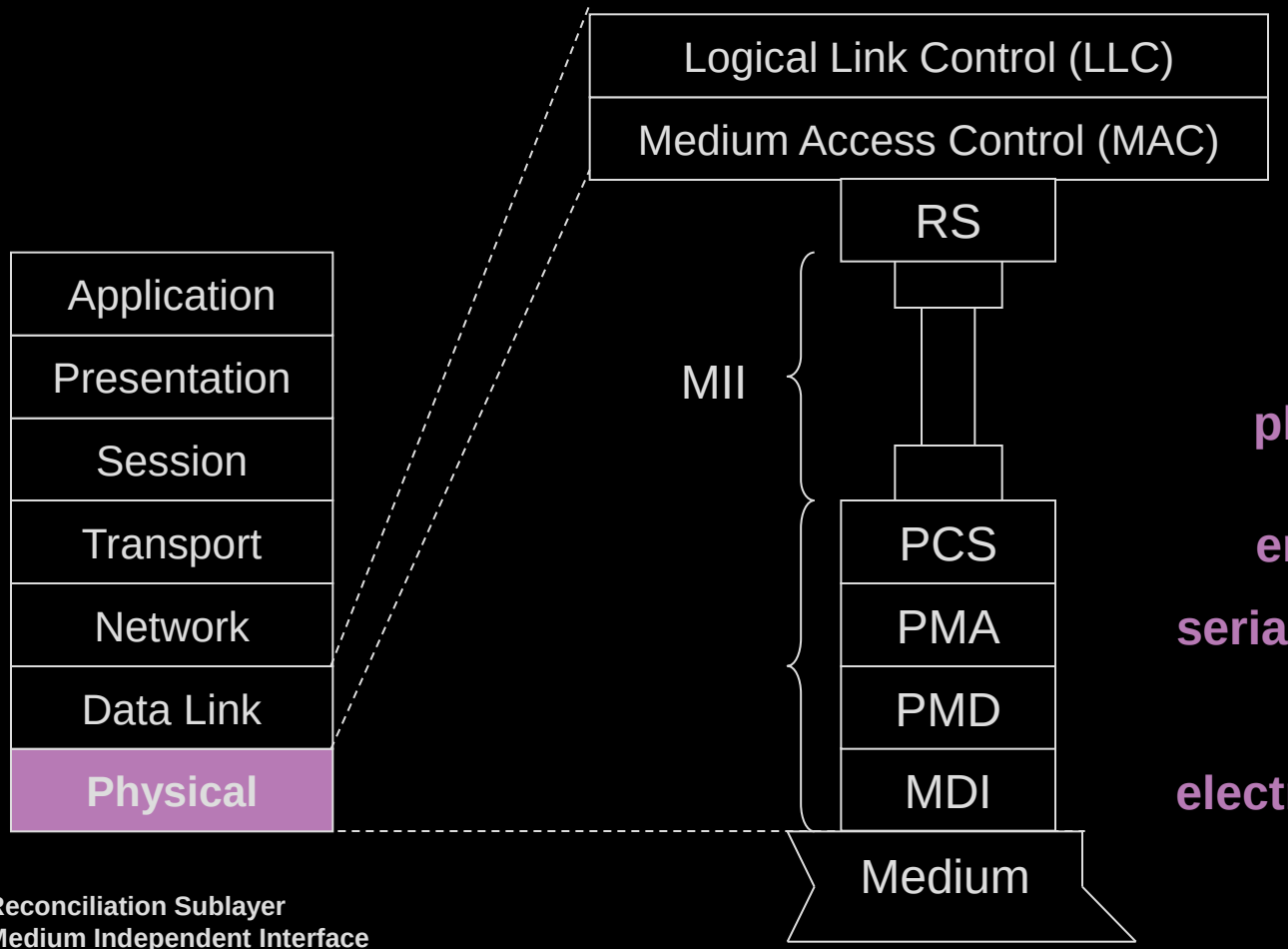
> Point-to-point distribution of timing signals in Ethernet environments
> Synchronize the physical layer as currently done in SONET/SDH
> Packetize Synchronization Status Messaging protocol (SSM)
> Bring carrier grade telecom quality clocks to Ethernet switches
> Implementation conformant with IEEE 802.3 specification
> High-level definition part of ITU-T G.8261 clause 8.1.1
> Specification to be established within ITU-T G.pacmod & G.paclock

Enabler to Carrier-Grade Ethernet

Synchronous Ethernet Applications

> Network timing distribution (migration from SDH/SONET)
> GSM & UMTS wireless backhaul
> Gigabit & Ethernet Passive Optical Networks (PON)
> Network/reference clock for differential timing technique
> Interworking with PDH/SDH/Ethernet microwave radios synchronization
> Interworking with Layer 2+ adaptive timing techniques
> Packet backplane interconnect
> Enable TDM/ATM pseudowires (CES)
> Achieve higher Ethernet data rates
> Enable location & sensor based services

IEEE 802.3 Standards Architecture (100BASE-TX)



mapping

interconnect
physical interface

encoding/decoding

serialization/clock recovery

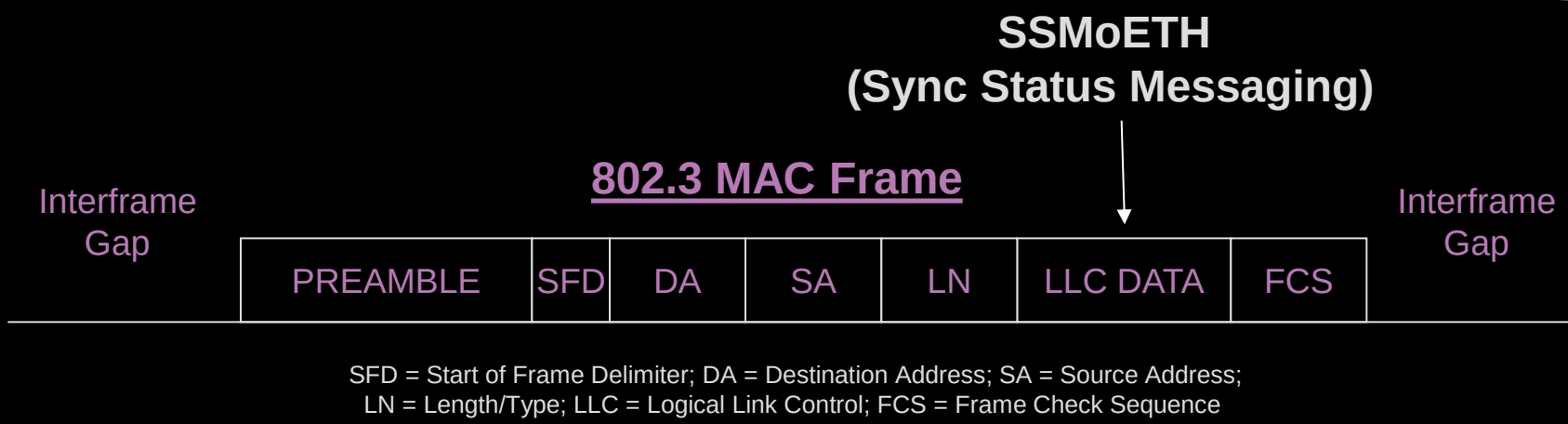
media types

electrical driver/connector

RS: Reconciliation Sublayer
MII: Medium Independent Interface
PCS: Physical Coding Sublayer
PMA: Physical Medium Attachment
PMD: Physical Medium Dependence
MDI: Medium Dependence Interface

Ref: IEEE Std. 802.3, Clause 21, Figure 21-1

- 802.3 MAC Frame
- 100BASE-TX Physical Layer Stream



SFD = Start of Frame Delimiter; DA = Destination Address; SA = Source Address;
LN = Length/Type; LLC = Logical Link Control; FCS = Frame Check Sequence

100 BASE-TX Physical Layer Stream

IDLE = [1 1 1 1….]
SSD = Start of Stream Delimiter = [1 1 0 0 0 1 0 0 0 1]
PREAMBLE = [1 0 1 0 ….] 62 alternating 1's and 0's
SFD = Start of Frame Delimiter [1 1]
DA, SA, LN, LLC DATA, FCS = [Data]
ESD = End of Stream Delimiter

Before/After 4B5B Encoding, Scrambling, and MLT3 Coding

802.3 MII Signals

> 16-pin signal interface to decouple MAC layer from the various PHY layers
> 7 transmit, 7 receive, 2 network status (excluding management pins)
> Nibble-wide (4 bits) transmit/receive interface for each clock cycle → 25MHz
> Transmit (TX_CLK) & Receive (RX_CLK) path can operate with different clocks

MII Signals		
Transmit	**Receive**	**Status**
Transmit clock (TX_CLK)	Receive clock (RX_CLK)	Carrier sense (CRS)
Transmit data (TXD[3:0])	Receive data (RXD[3:0])	Collision (COL)
Transmit enable (TX_EN)	Receive data valid RX_DV)	
Transmit error (TX_ER)	Receive error (RX_ER)	

MII – Media Independent Interface

Ref: IEEE Std. 802.3, Clause 22.2

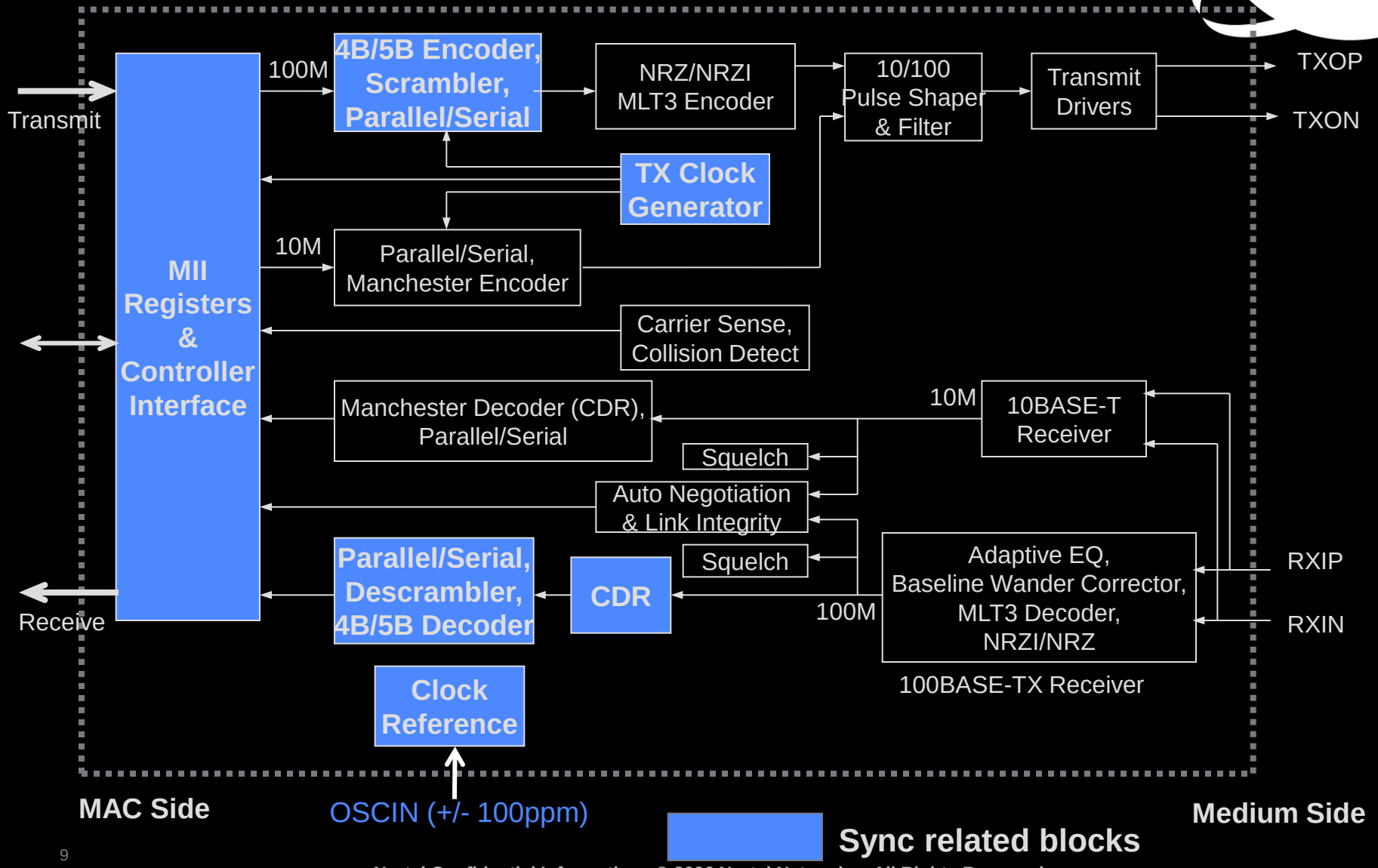
RMII Signals

> Reduced MII to overcome number of signal pins for high port density designs
> Vendor agreement specification, 6 or 7-pin signal interface
> Di-bits wide (2 bits) each clock cycle → 50MHz reference clock
> Transmit/Receive path synchronous to reference clock

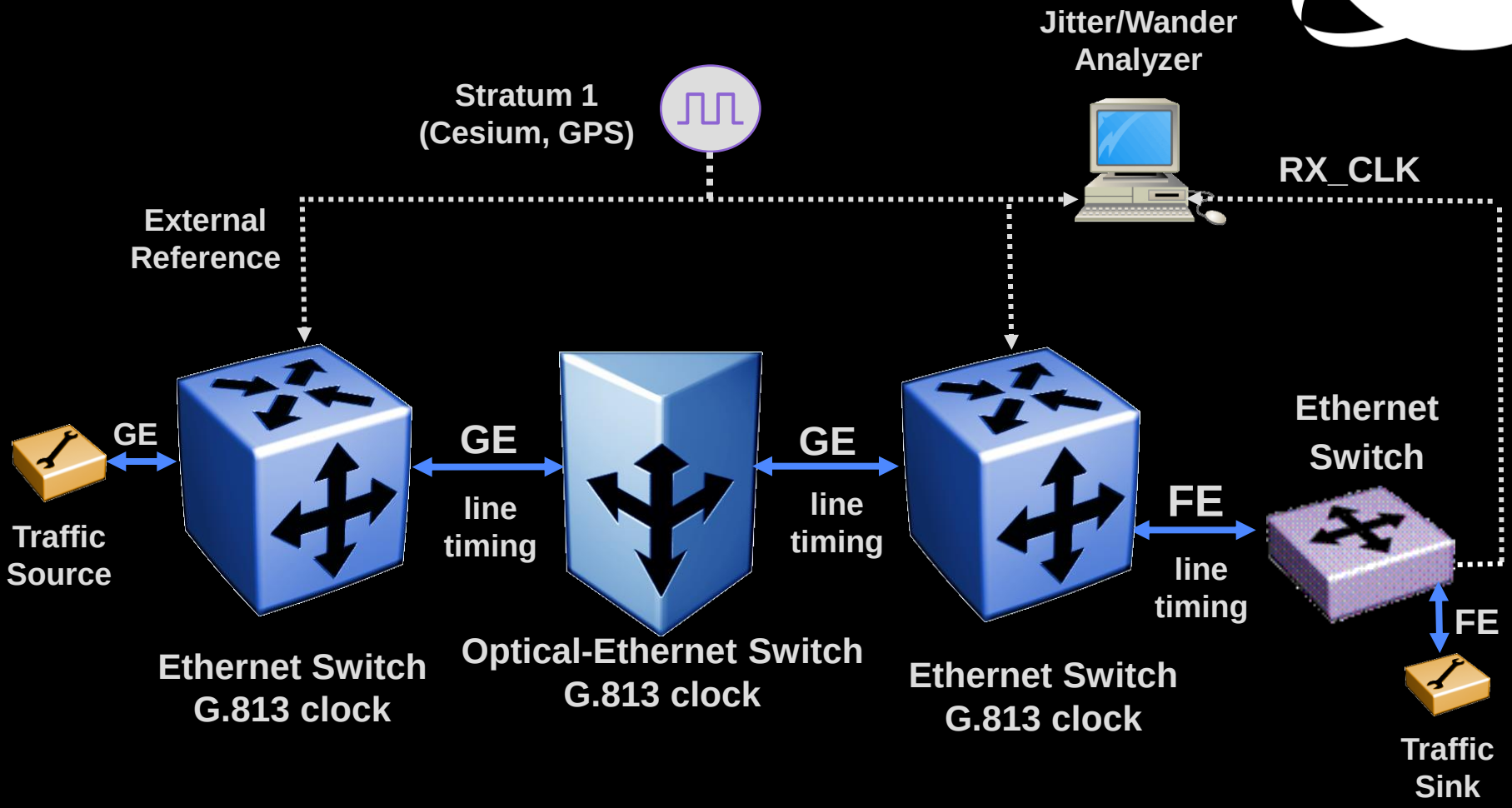
RMII Signals
Reference clock (REF_CLK)
Carrier Sense / Receive data valid (CRS-DV)
Receive data (RXD[1:0])
Transmit enable (TX_EN)
Transmit data (TXD[1:0])
Receive error (RX_ER)

No recovered clock available from RMII signals

Internals of a Typical 100BASE-TX PHY /1



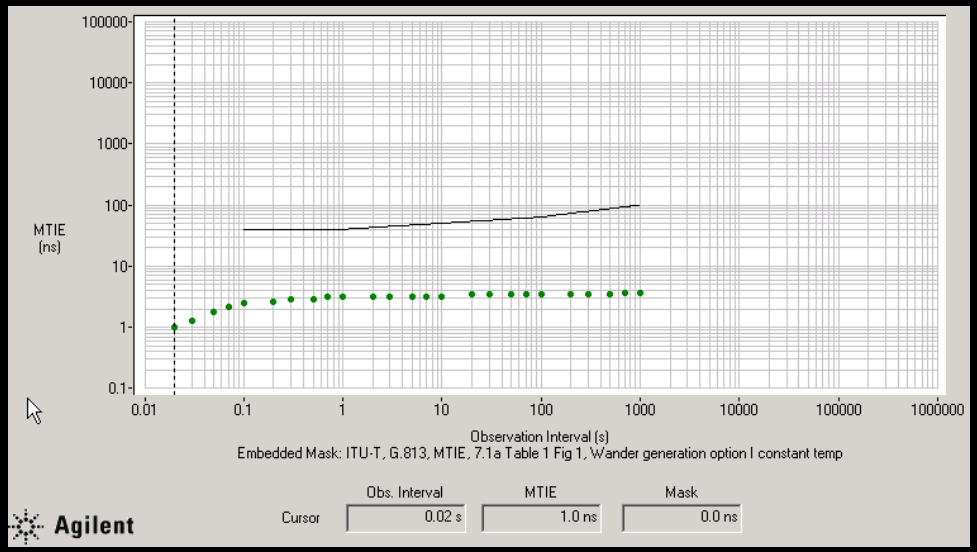
Experimental Setup



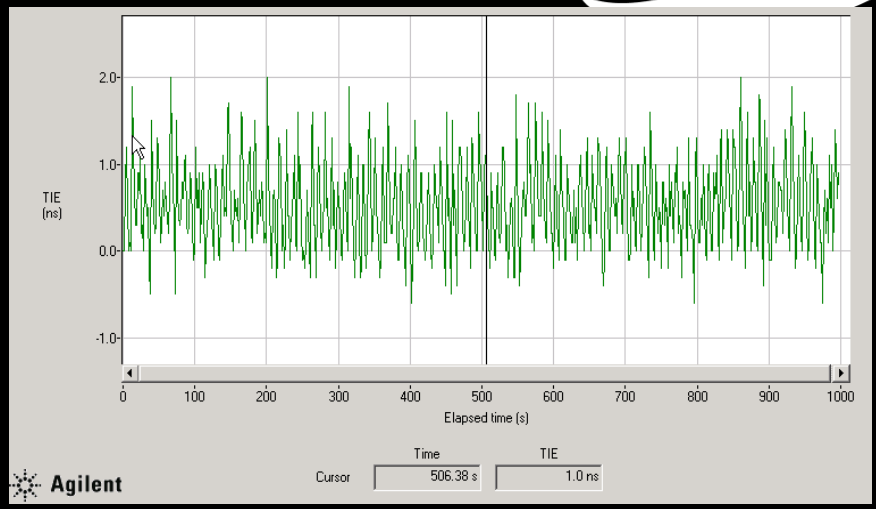
Synchronous Ethernet Domain

G.813 SEC Noise Generation

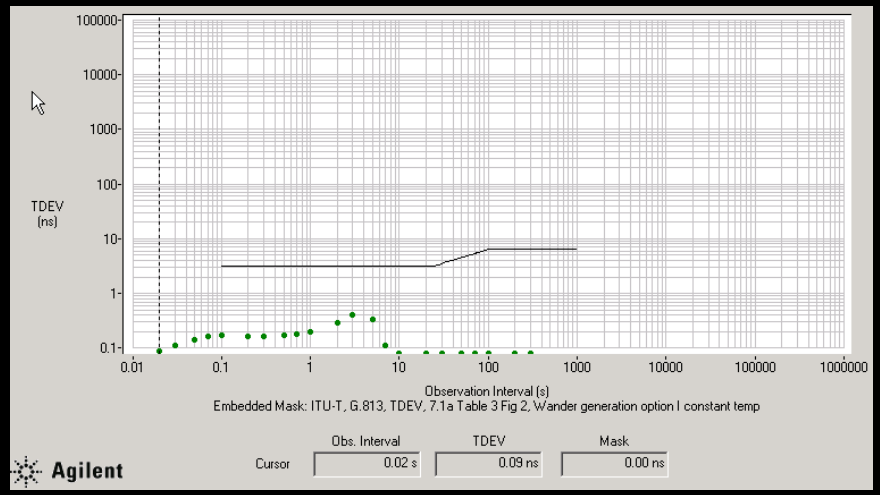
> Measure clause 7.1 wander in locked mode
> Still some MTIE & TDEV margin left



MTIE



TIE



TDEV

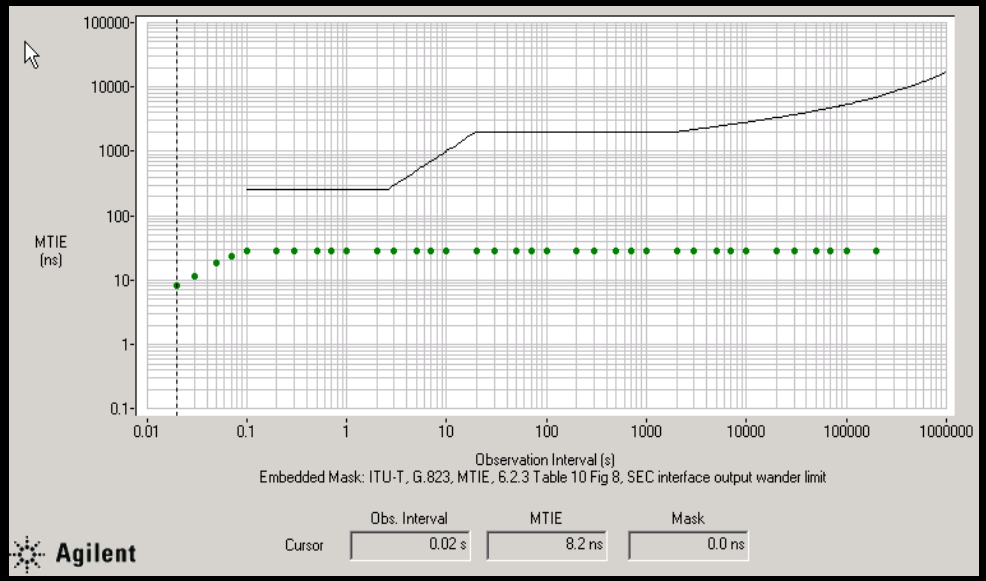
G.823 SEC Interface Output Wander

- **Locked mode (Line Timing)**

> Measure output wander for 3 days

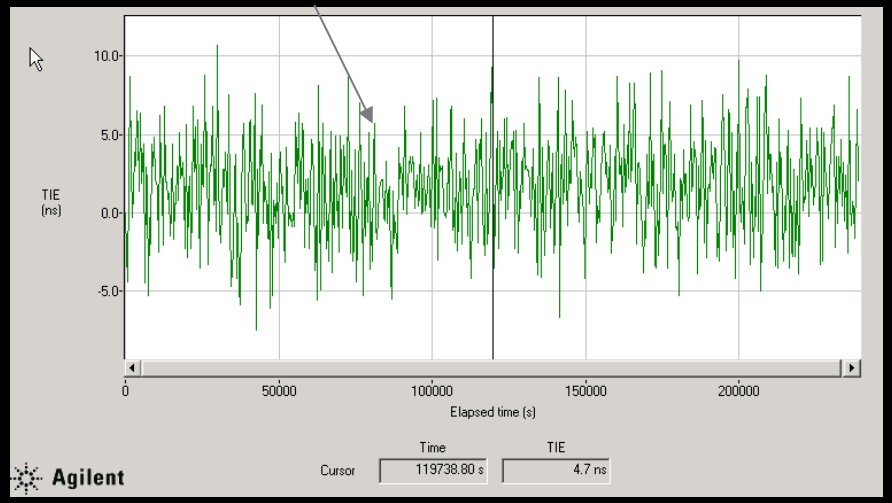
> Lots of MTIE margin left

> Could tolerate many more hops

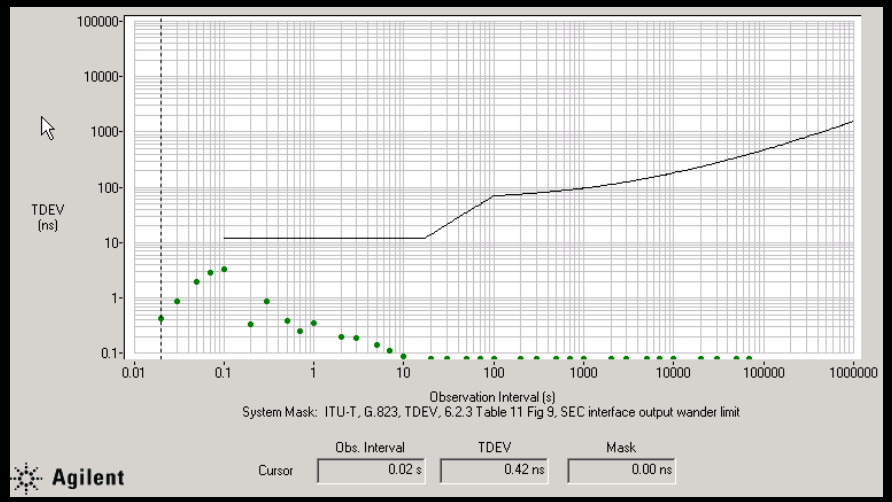


MTIE

G.813 10Hz bandwidth used
Can be lowered to further reduce TIE



TIE



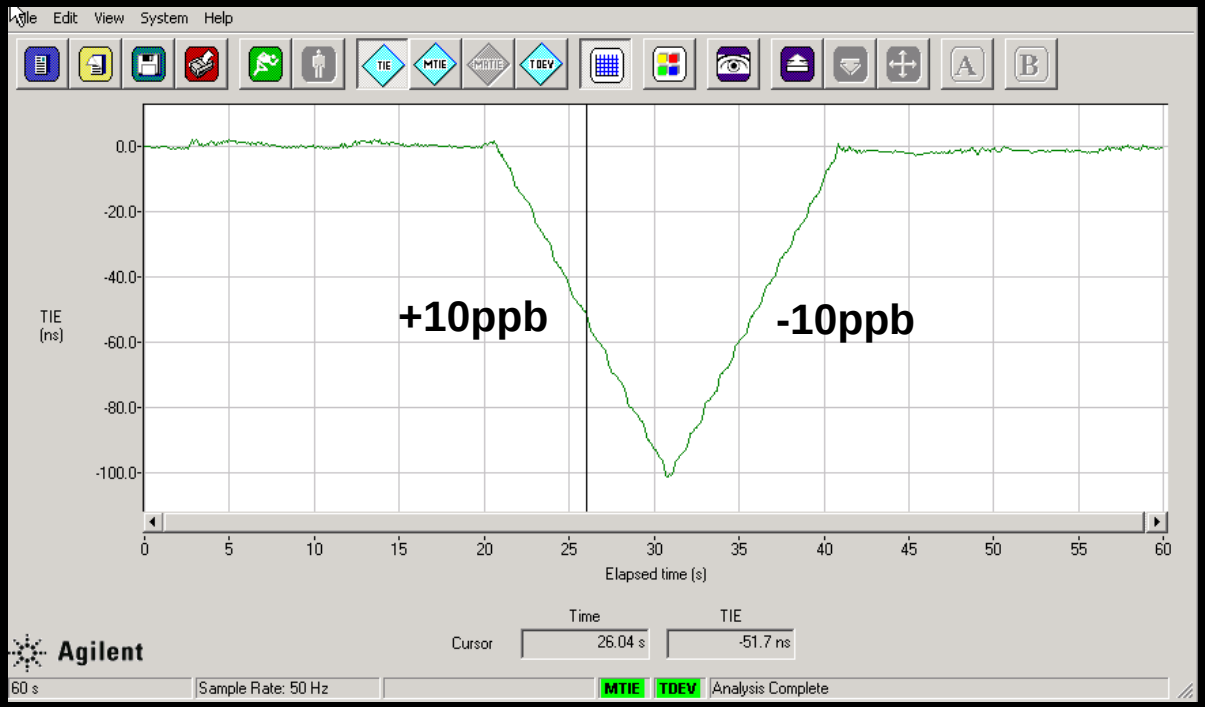
TDEV

Frequency Offset

> Introduce +10ppb from 20 to 30 seconds

> Introduce -10pbb from 30 to 40 seconds

> Ethernet PHYs are fast at acquiring & locking to offsets



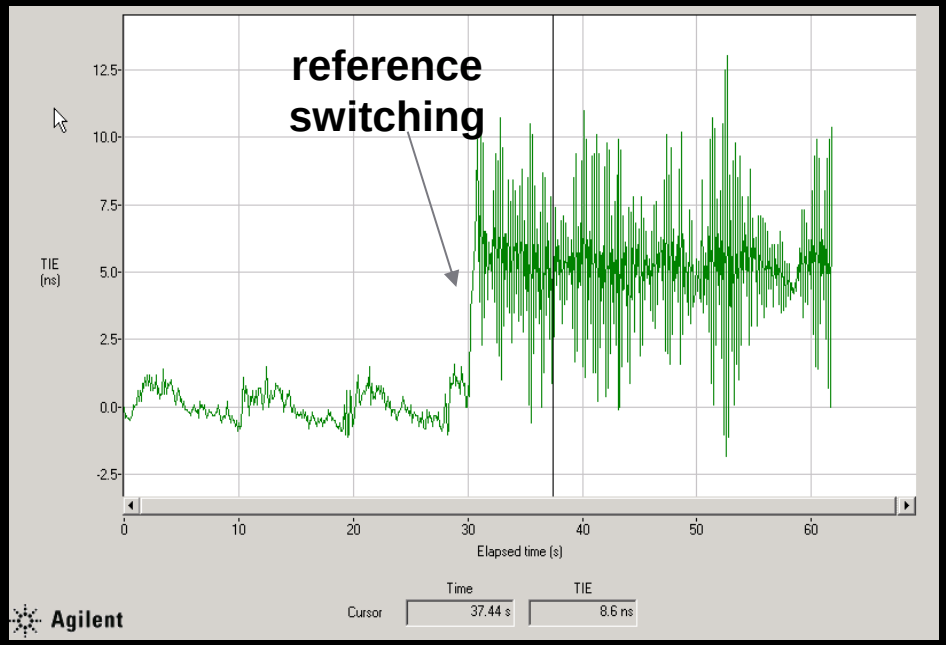
TIE

G.813 Short-term Phase Transient Response
- Reference switching

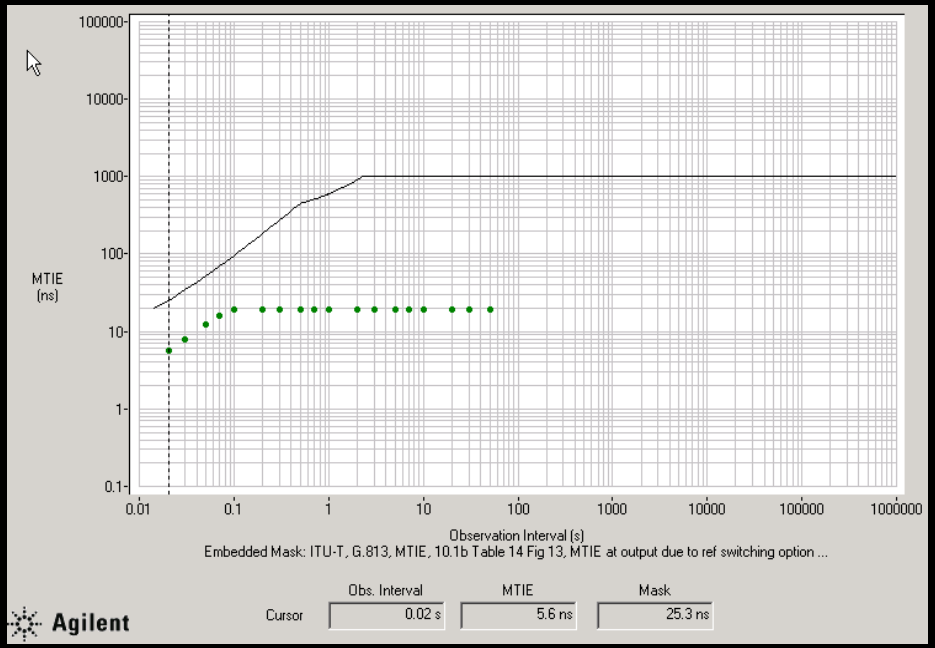
> Disconnect external reference (into last switch)

> Clock rearrangement (reference switching) to line timing reference

> Measure against clause 10.1 option 2 (also within requirement for option 1)



TIE

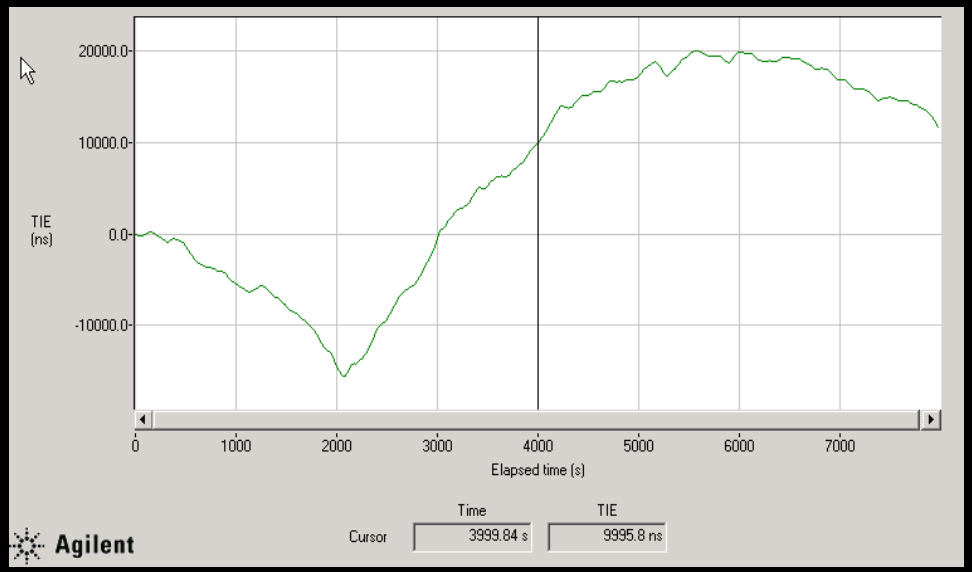


MTIE

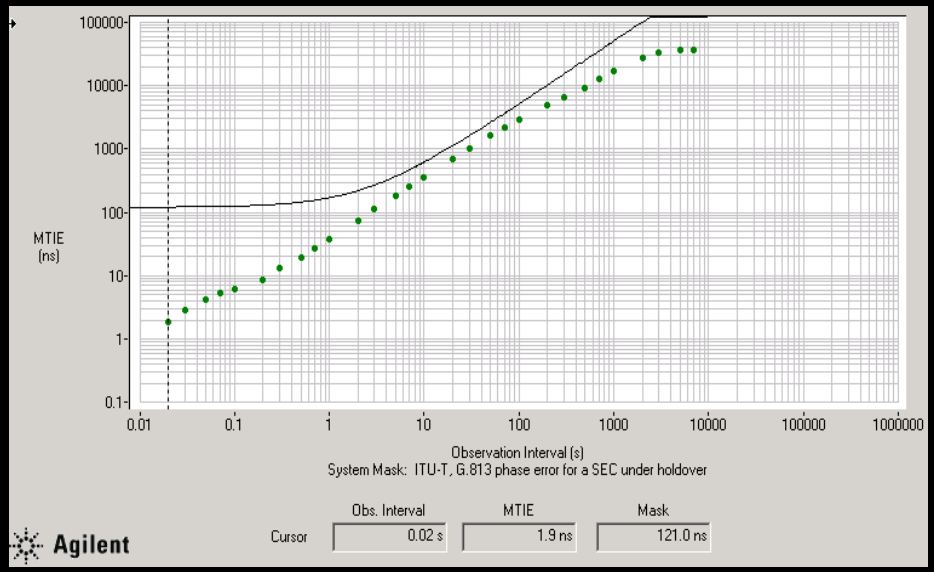
G.813 Long-Term Phase Transient Response
- Holdover

> Disconnect all timing references (external + line) going into the last G.813 clock

> Measure against clause 10.2 holdover mask specification



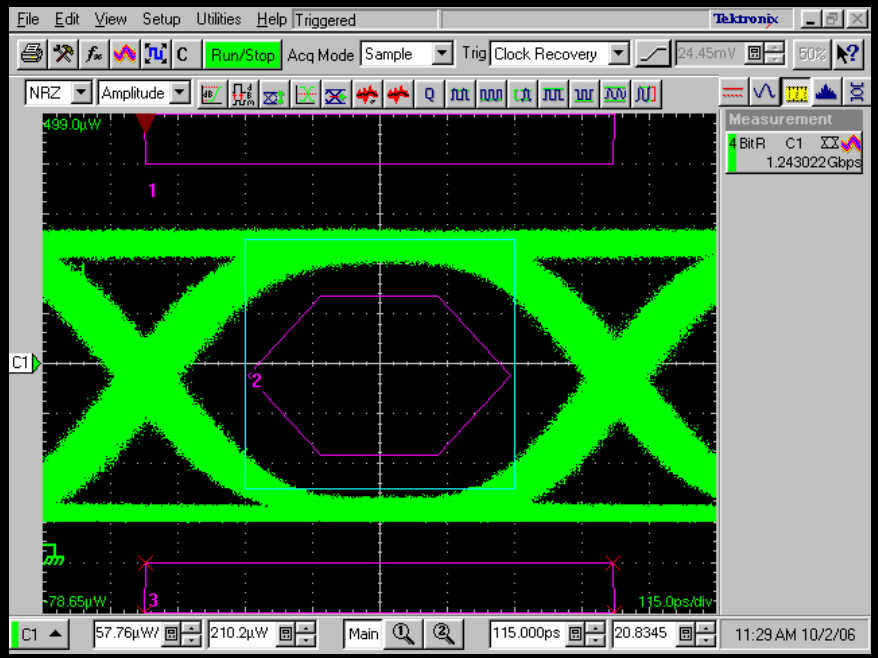
TIE



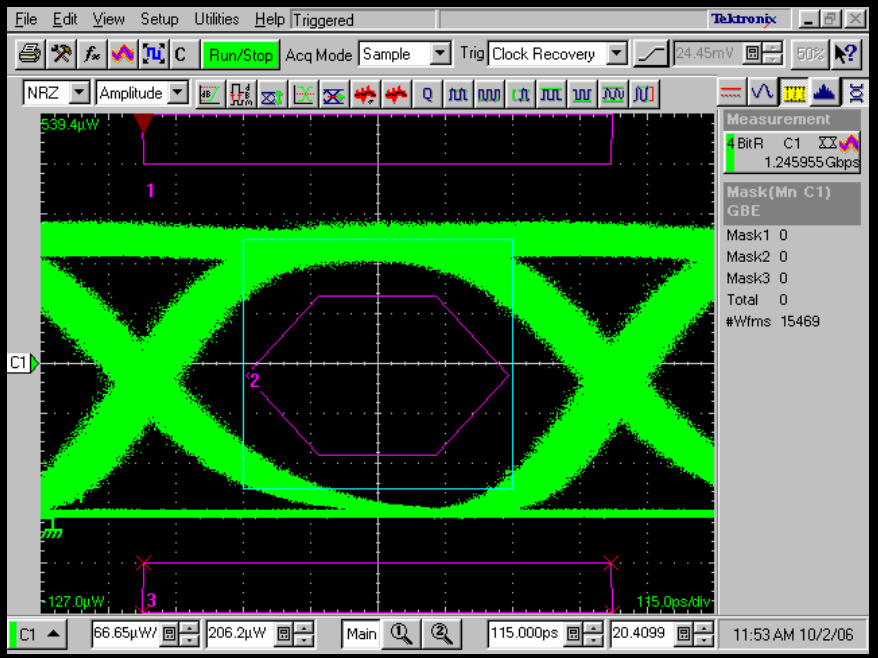
MTIE

IEEE 802.3 Transmitter Eye Mask

- Measure transmitter eye diagram at a SyncE 1000BASE-SX interface
- Follow IEEE 802.3 clause 38.6.5 (optical measurement guidelines)
- Still some margins left before exceeding the transmitter pulse shape mask



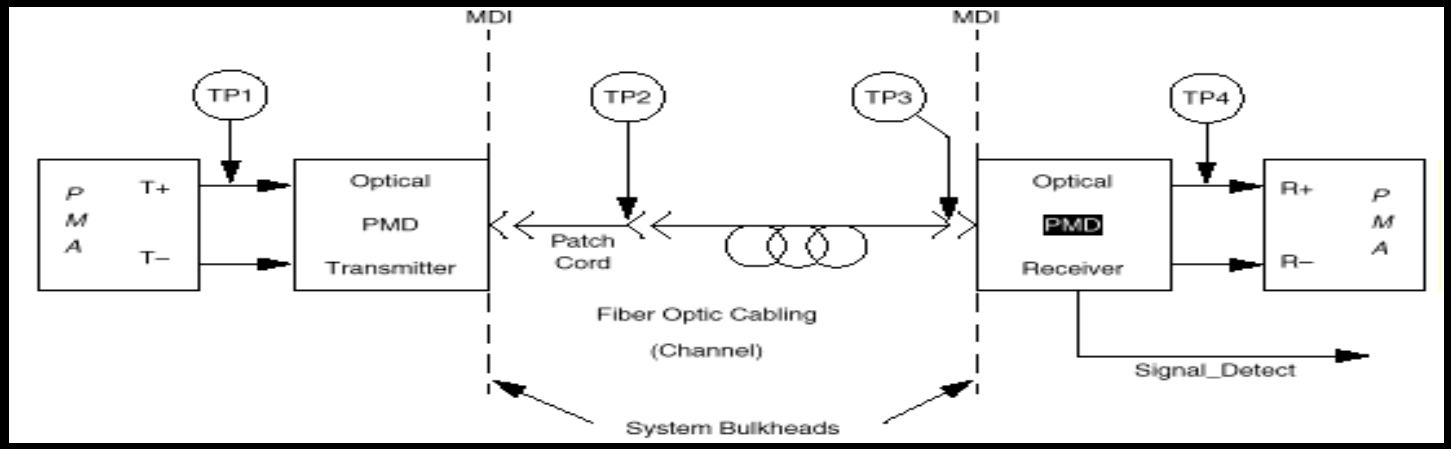
TX Switch 1



TX Switch 2

IEEE 802.3 Jitter

- Measure jitter at a SyncE 1000BASE-SX interface
- Follow IEEE 802.3 clause 38.5 (Jitter specification)
- Within jitter specification



Jitter budget at Compliance point TP2		
	Deterministic Jitter	**Total Jitter**
Specification	160 nsec	345 nsec
Measured	48 nsec	228 nsec

Summary

> Native-Ethernet switch having SDH/SONET synchronization properties

> It was shown that a G.813 clock, at minimum, is suitable for network timing distribution through native-Ethernet switches

> Ethernet data integrity fully preserved during testing

> PMO of IEEE 802.3 PHYs have most of the functions required

> No major sync-related differences between FE, GE and 10GE

> Synchronous Ethernet interfaces do not seem to impact IEEE 802.3 transmitter eye diagram & IEEE 802.3 jitter → ITU SG15/Q13 to investigate

> Technology has merit and will be driven by market demand