

Differential Timing Methods for Circuit Emulation

Ron Cohen
CTO – Resolute Networks

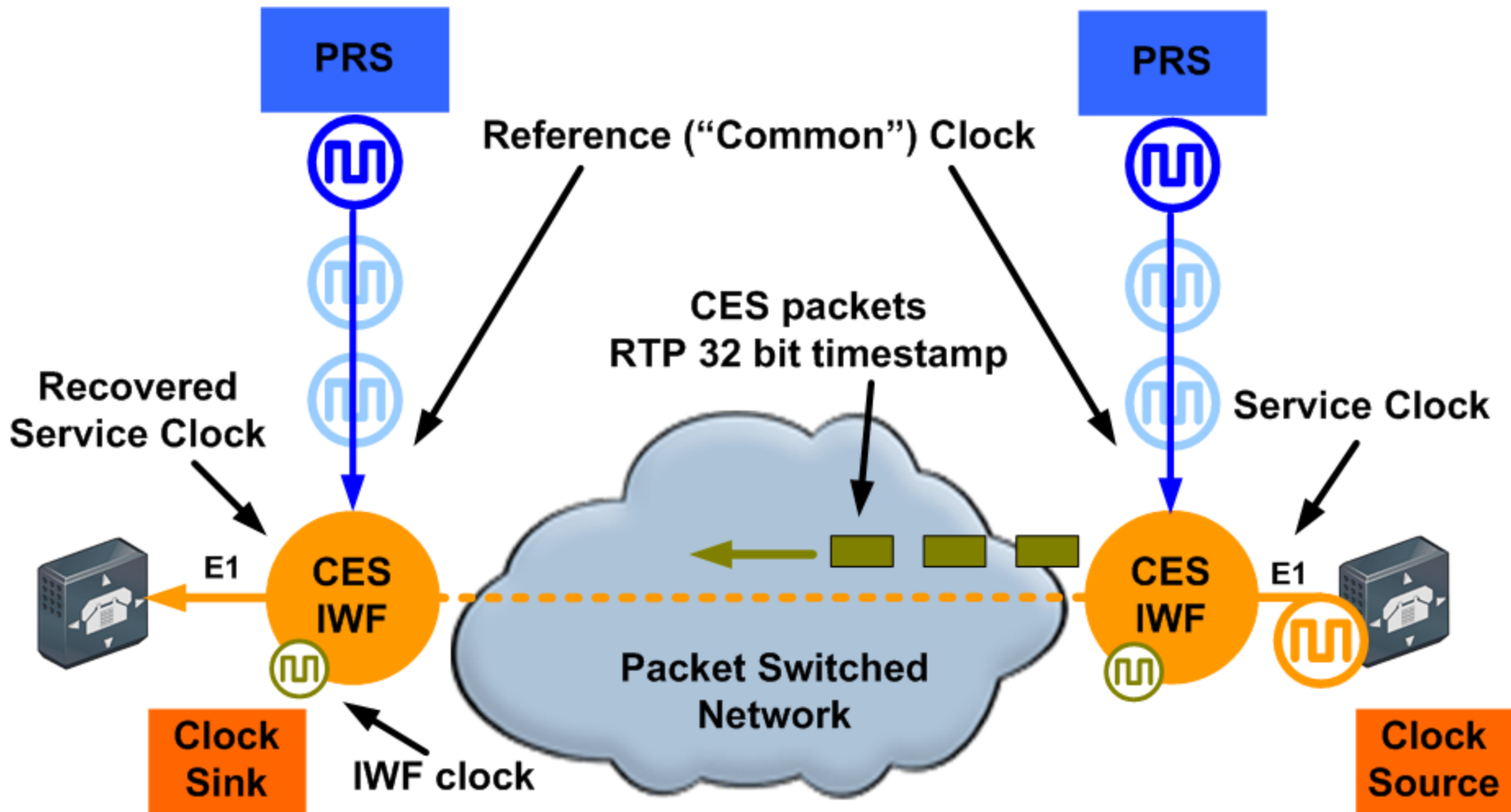
ronc@resolutenetworks.com

ITSF 2006

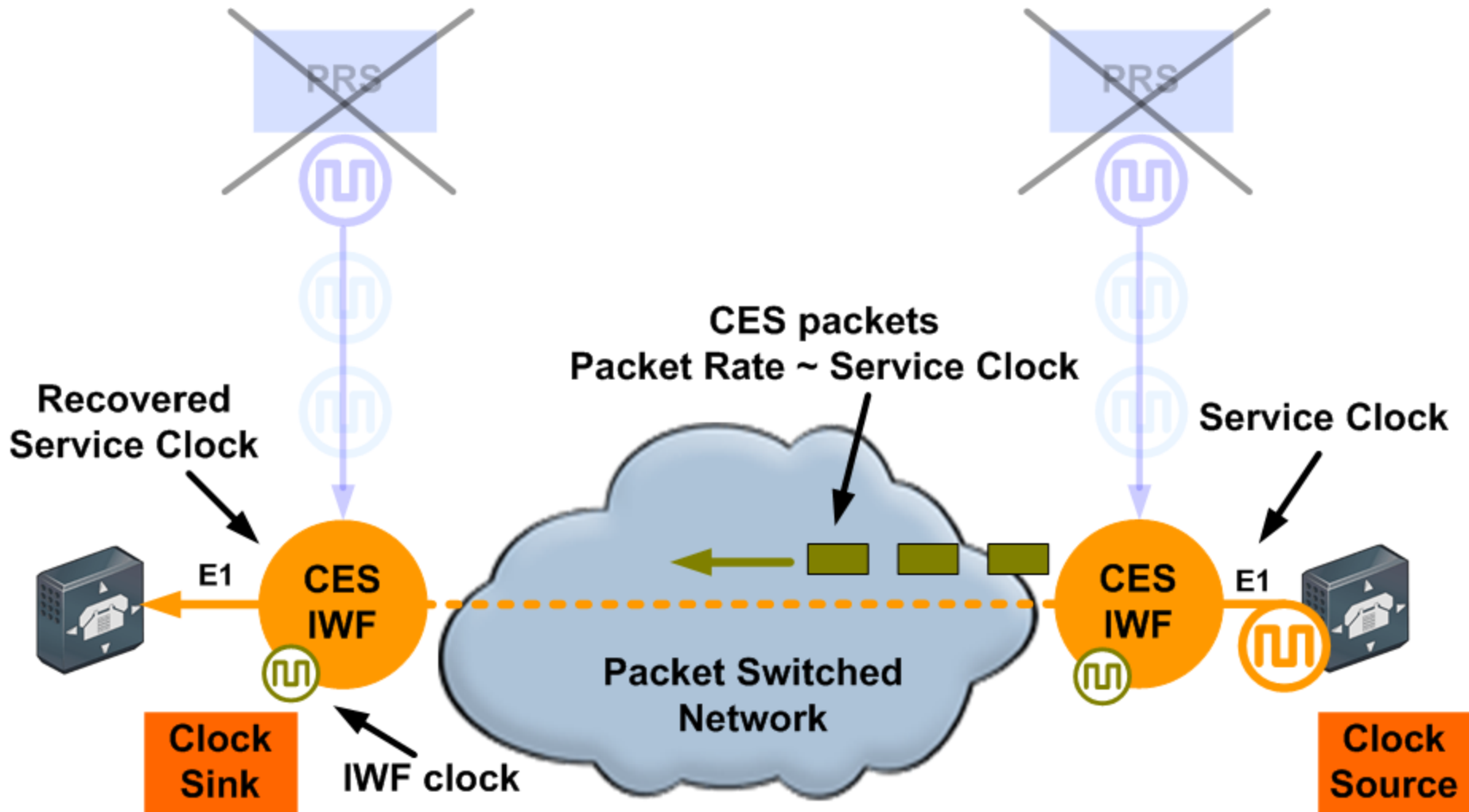
Agenda

- What is Circuit Emulation and what is Differential Timing all about?
- Deployment Scenarios Examples
- Requirements
- Differential Timing Performance Results from our Lab
- Combined Differential Timing and Synchronous Ethernet Lab Results

CES Differential Timing



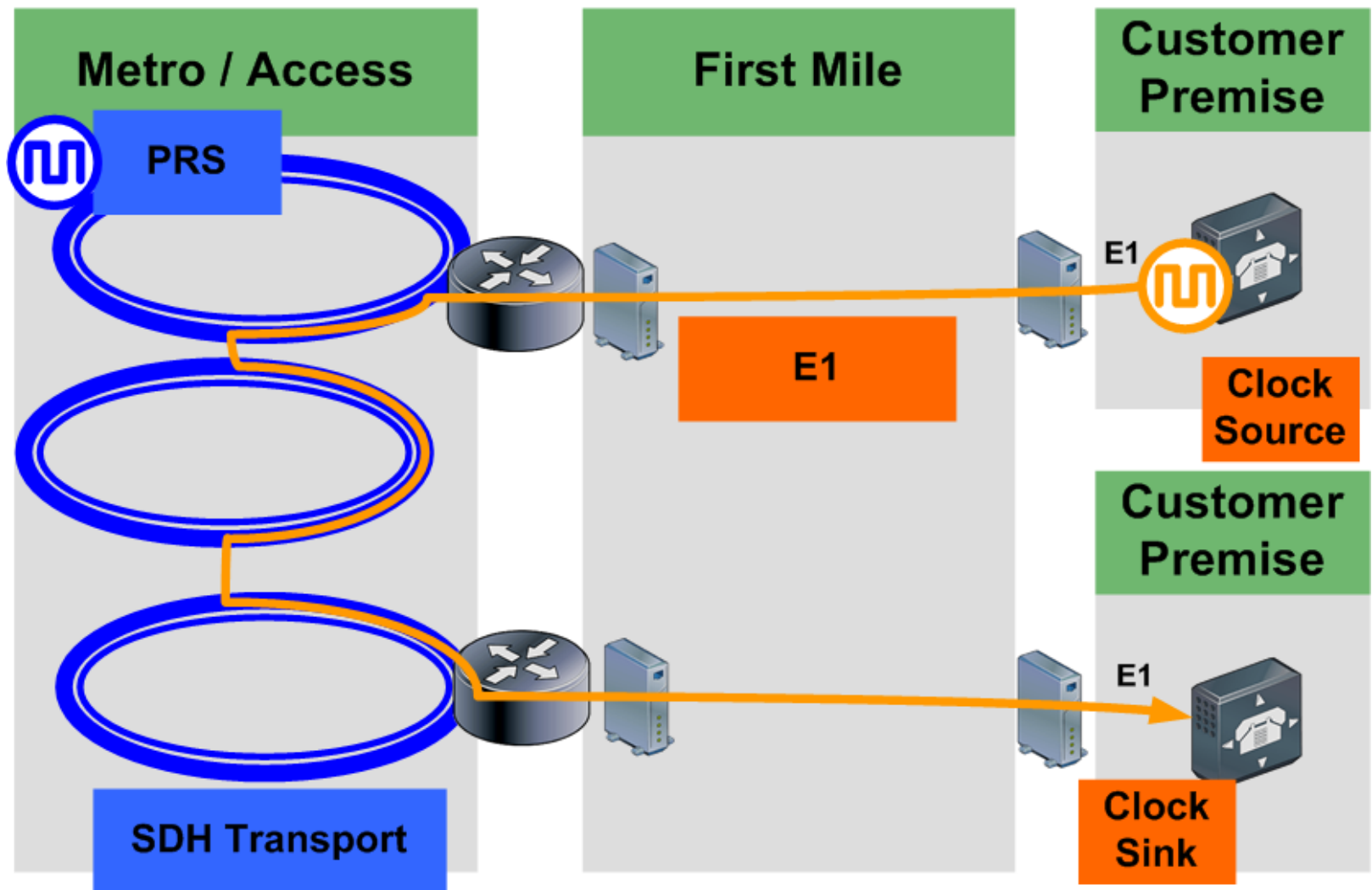
CES Adaptive Timing



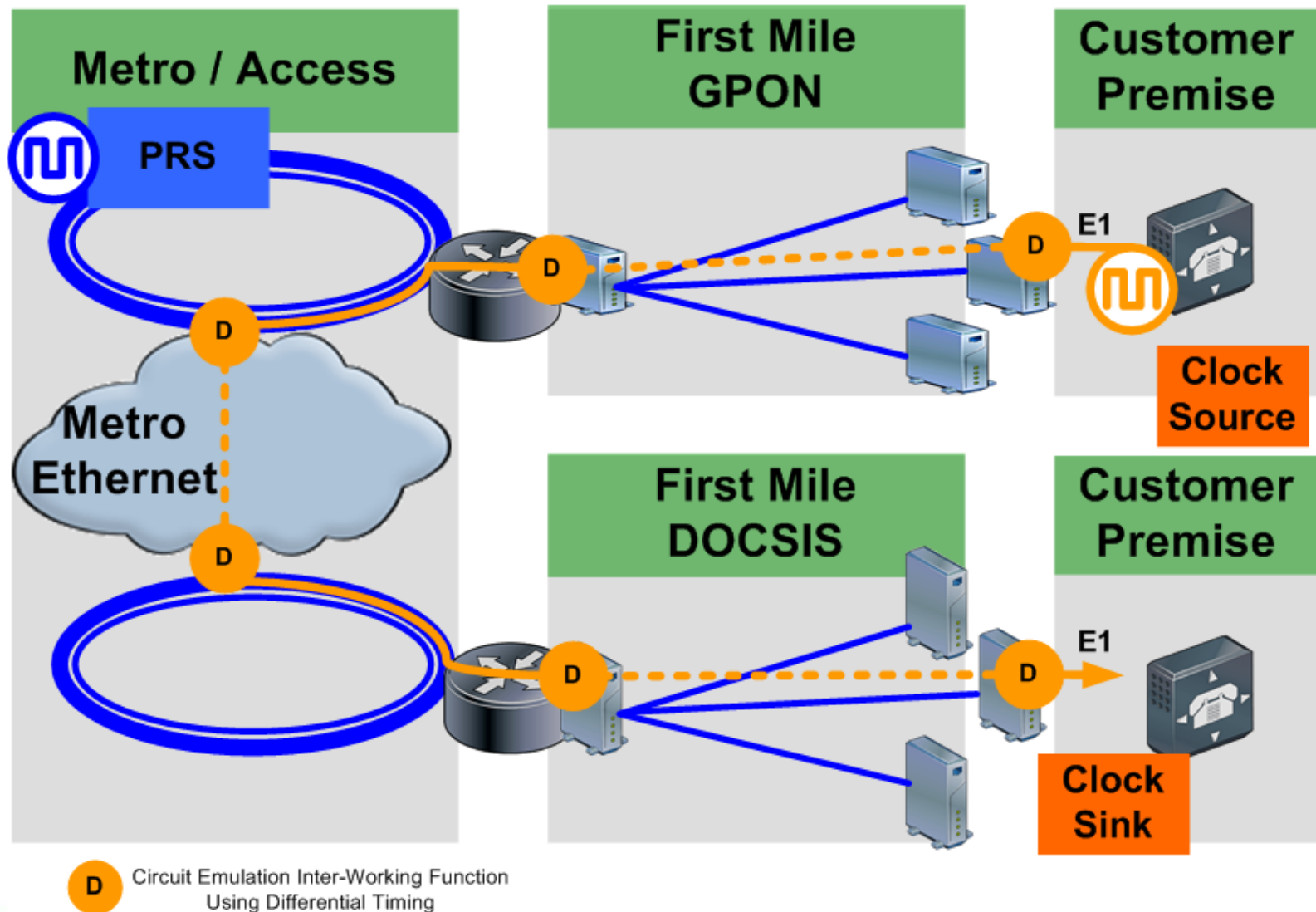
Differential vs. Adaptive

- Differential Timing Pros:
 - Handles well
 - Packet Switched Network (PSN) impairments, and in particular Packet Delay Variation (PDV)
 - Systematic PSN PDV due to beating effects
 - Faster settling time compared to Adaptive
 - Lower requirements for stability of IWF oscillator - leading to potentially cheaper solution with smaller footprint and power requirements
- Differential Timing Cons:
 - Requires Common Reference Clock

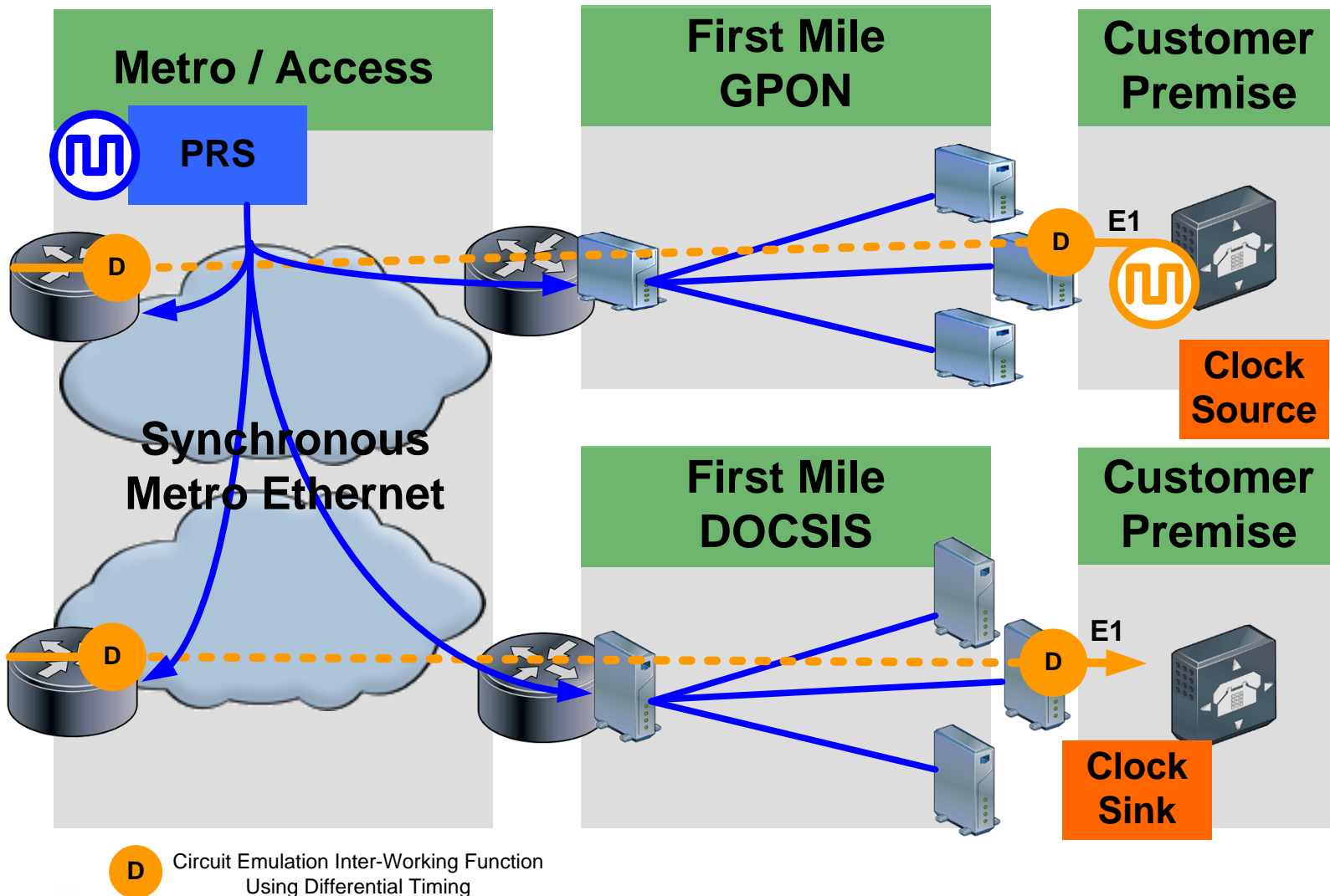
TDM Transport



Synchronous First Mile



Synchronous Metro Ethernet



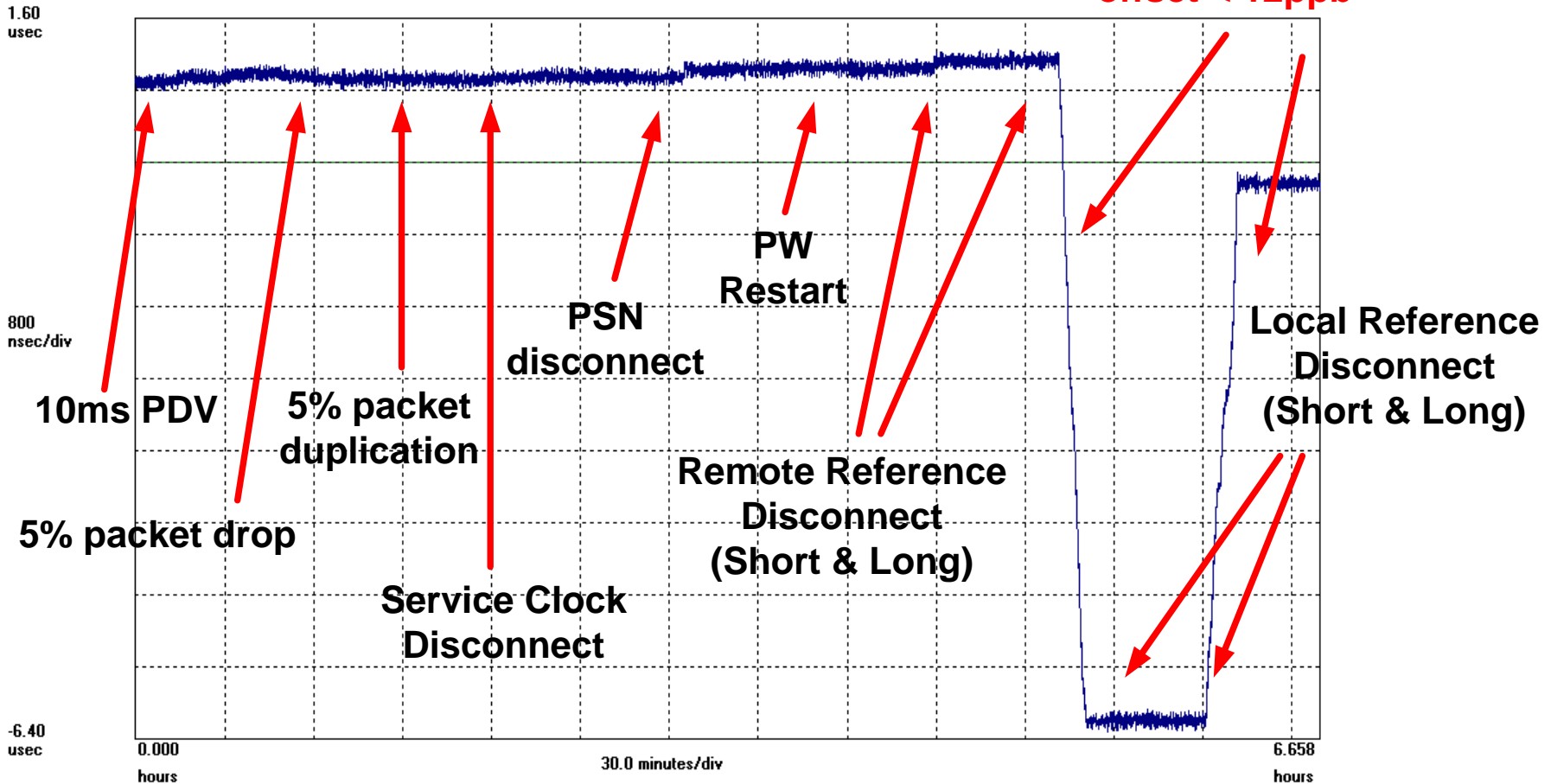
Requirements

- Wander MTIE compliance as specified in G.8261
 - consistent results across all
 - service clock frequencies
 - relevant common clock frequencies
- Robust to impairments introduced by
 - packet switched network
 - reference clock
 - service clock
- Mid-range performance IWF oscillator and peripherals

TIE: Impairments

Phase deviation in units of time; $F_s=9.012$ Hz; $F_o=1.5440000$ MHz; *7/27/2006 10:42:42 AM*; *7/27/2006 5:22:10 PM*;
HP 53132A; Test: 66; FB3; Samples: 216007; Fast Sampling; Ref ch1; TI/Time Data Only; TI 1->2;
FB3

**Holdover Frequency
offset < 12ppb**

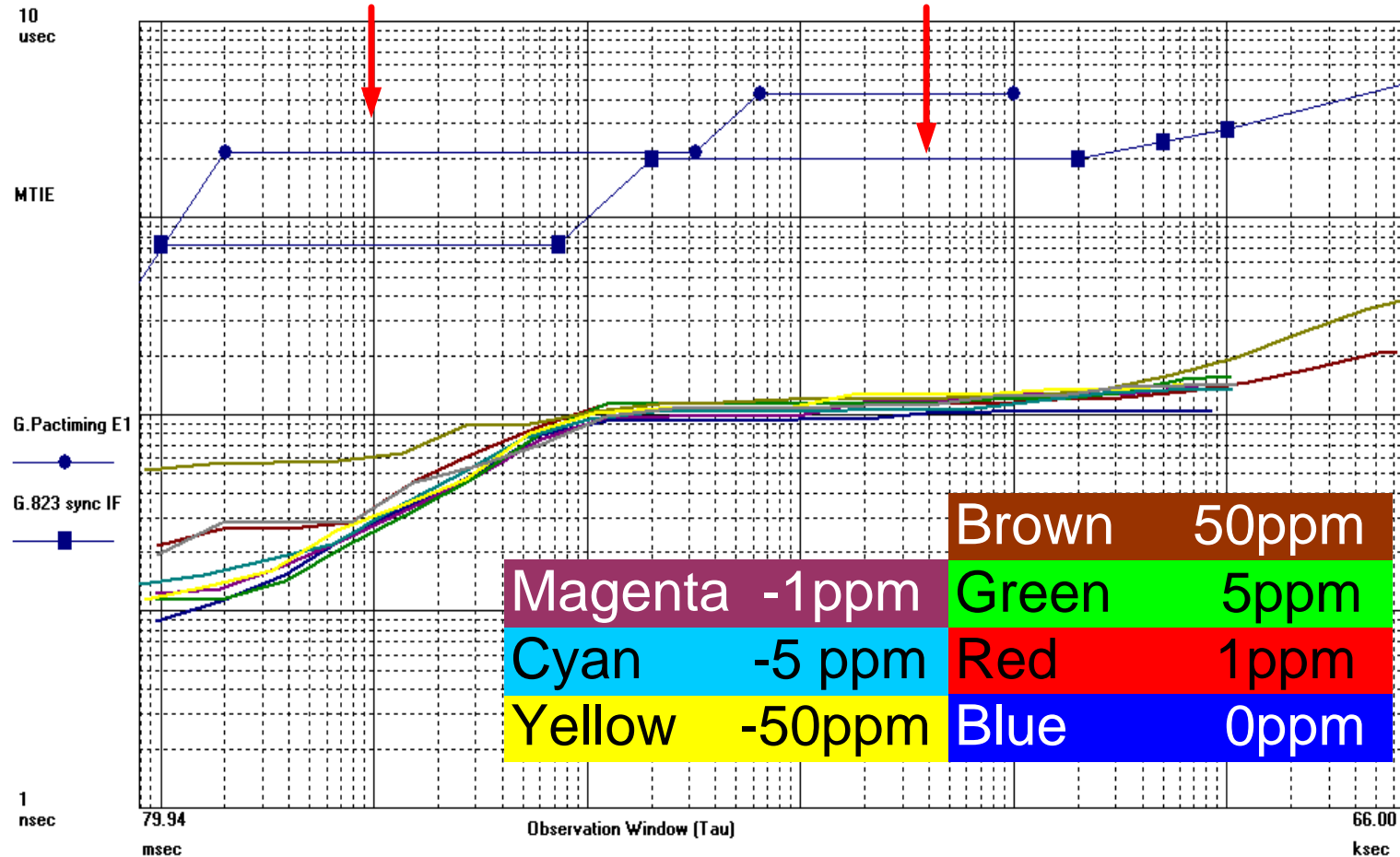


T1, CC=10.24MHz, TCXO

MTIE: Service Clock Dependency

G.8261 case 1

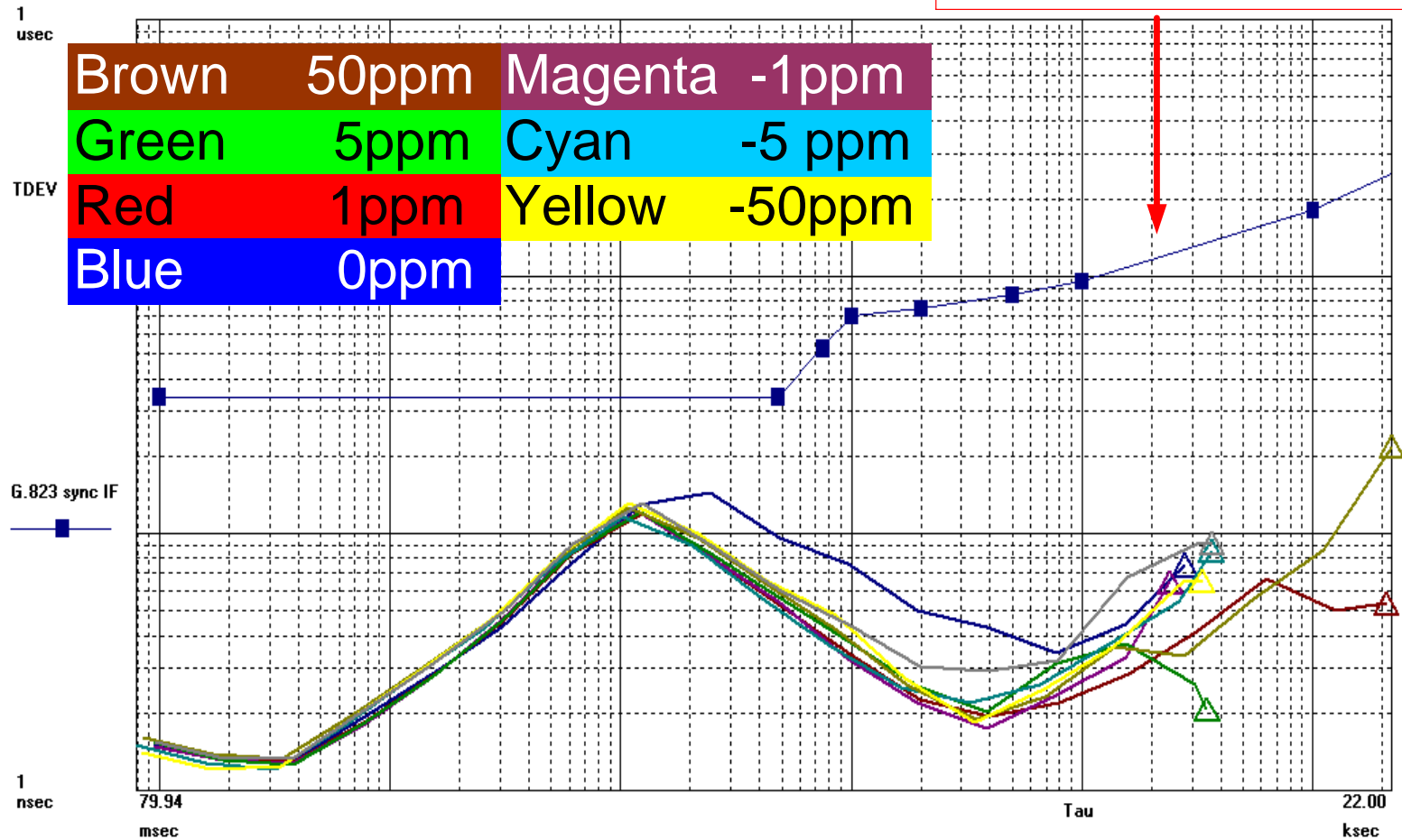
G.823 Sync Intrf.



E1, CC=16.384MHz, TCXO

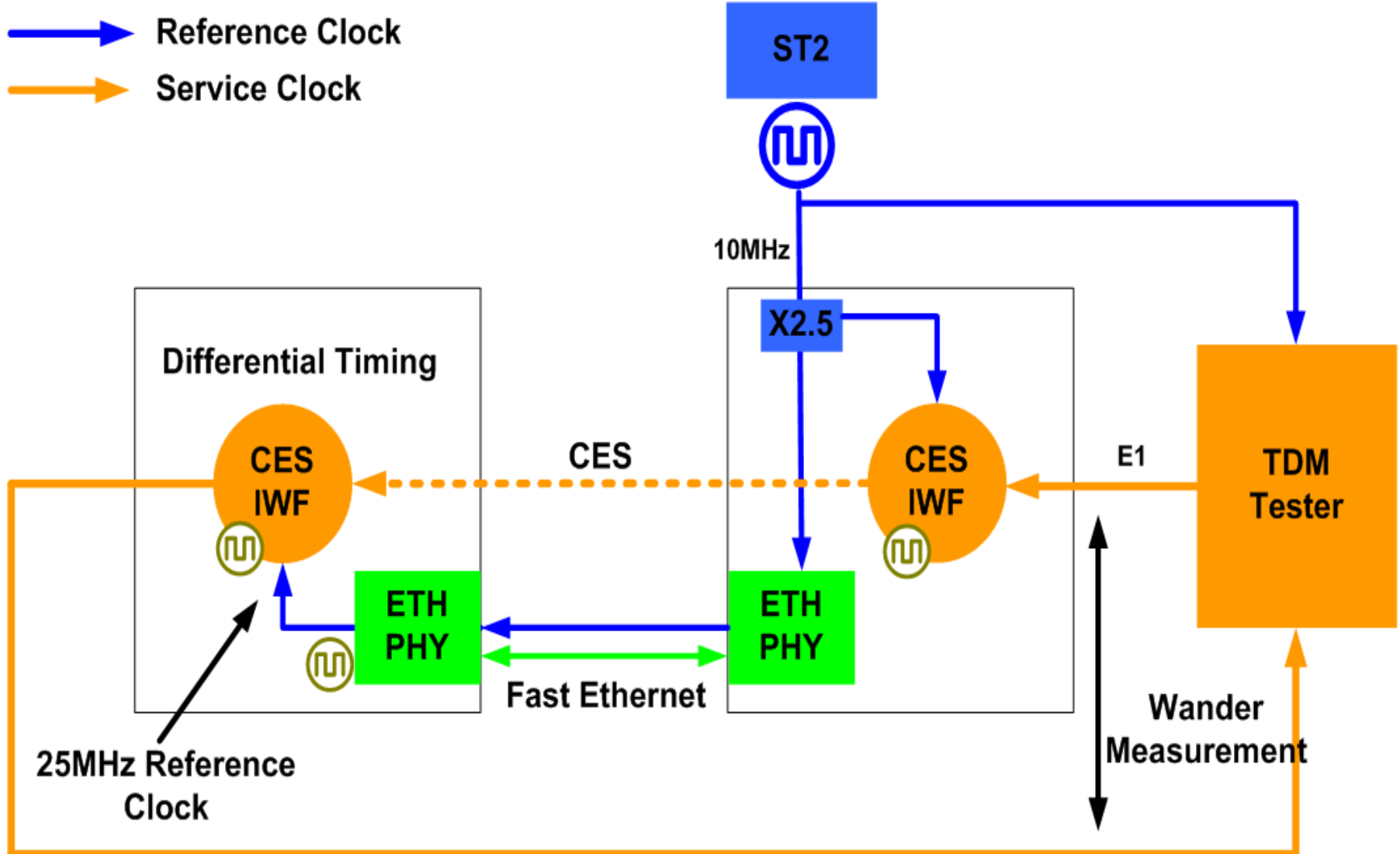
TDEV: Service Clock Dependency

G.823 Sync Infrf.

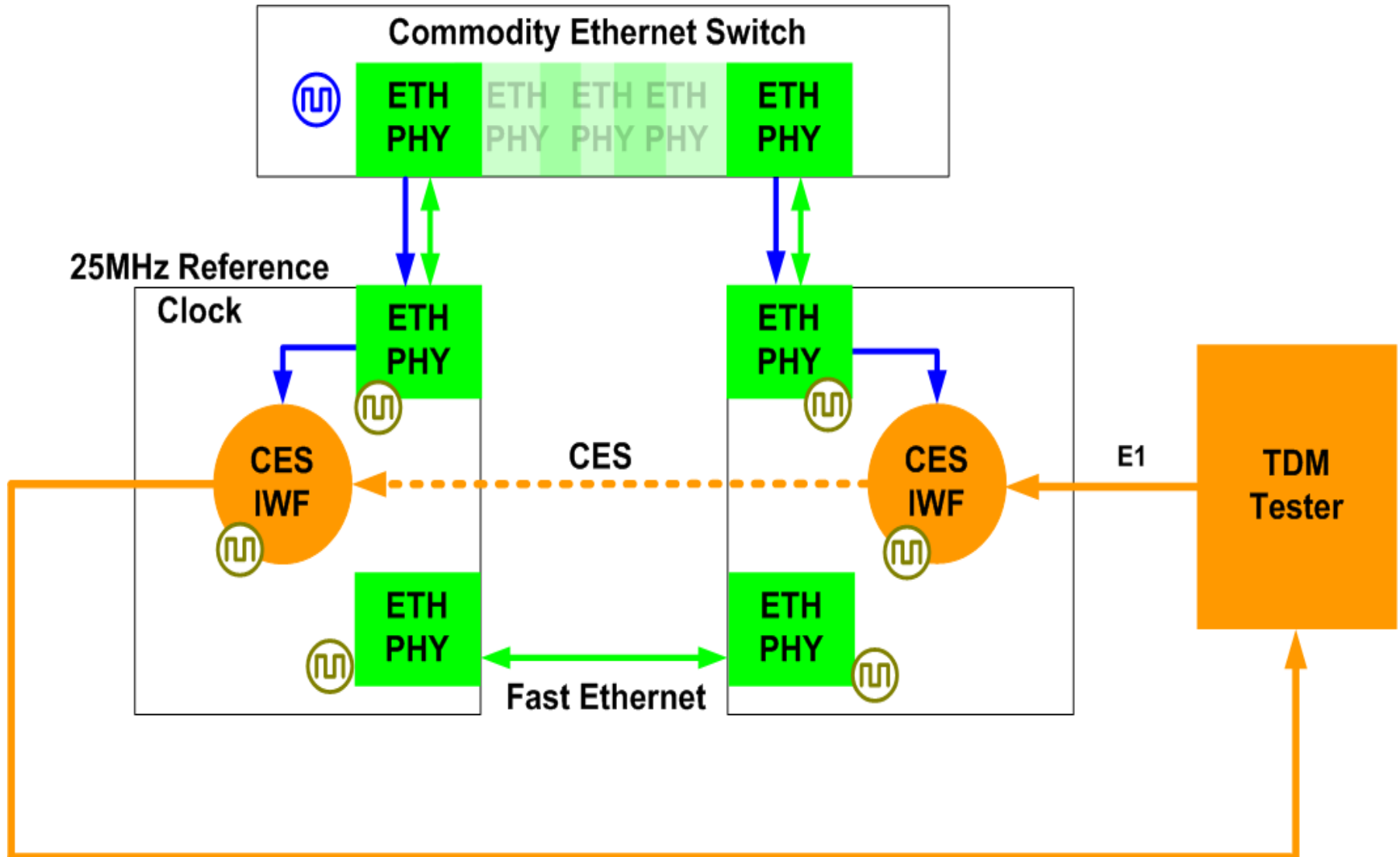


E1, CC=16.384MHz, TCXO

Sync Ethernet Setup A



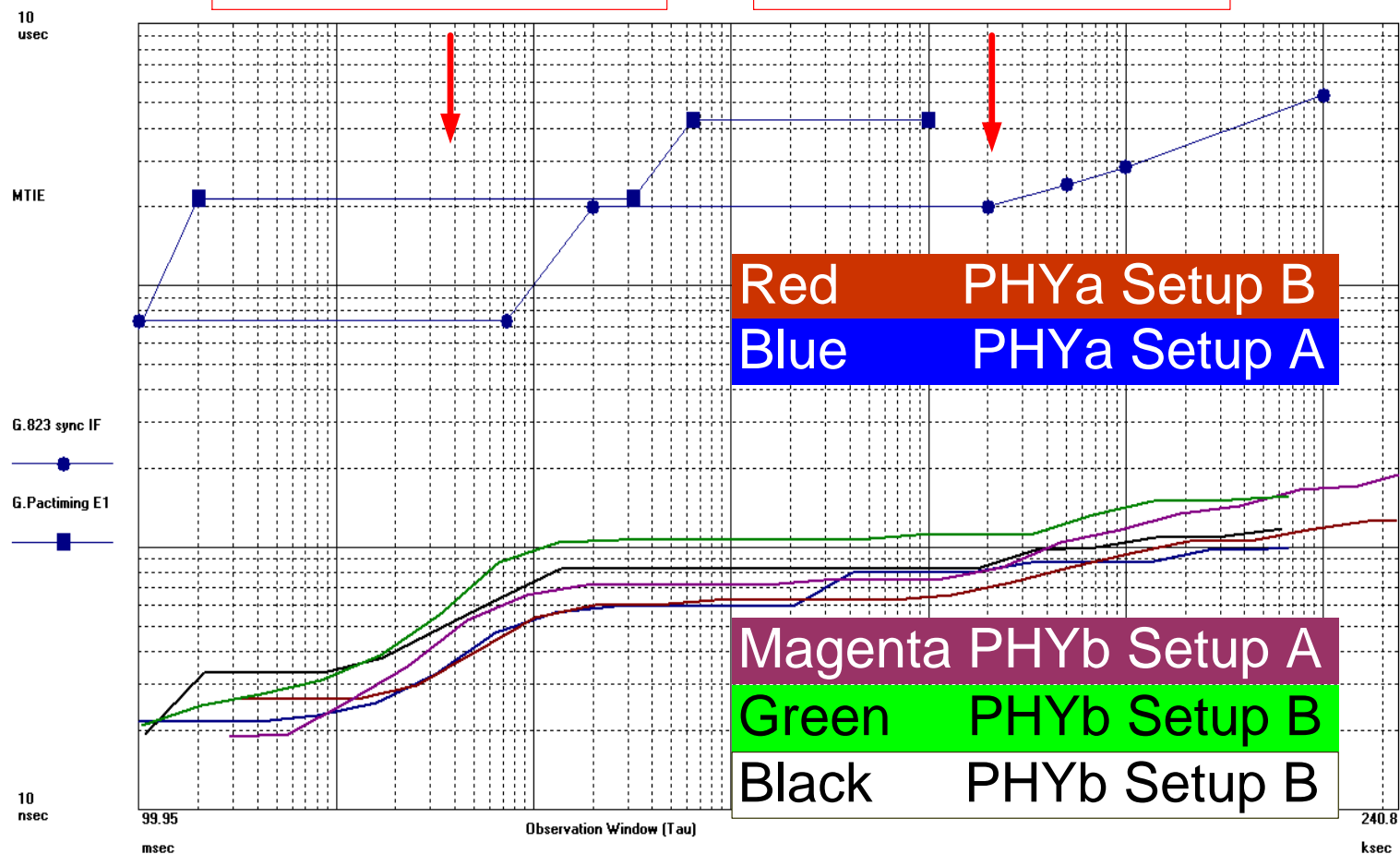
Sync Ethernet Setup B



MTIE: Sync Ethernet Results

G.8261 case 1

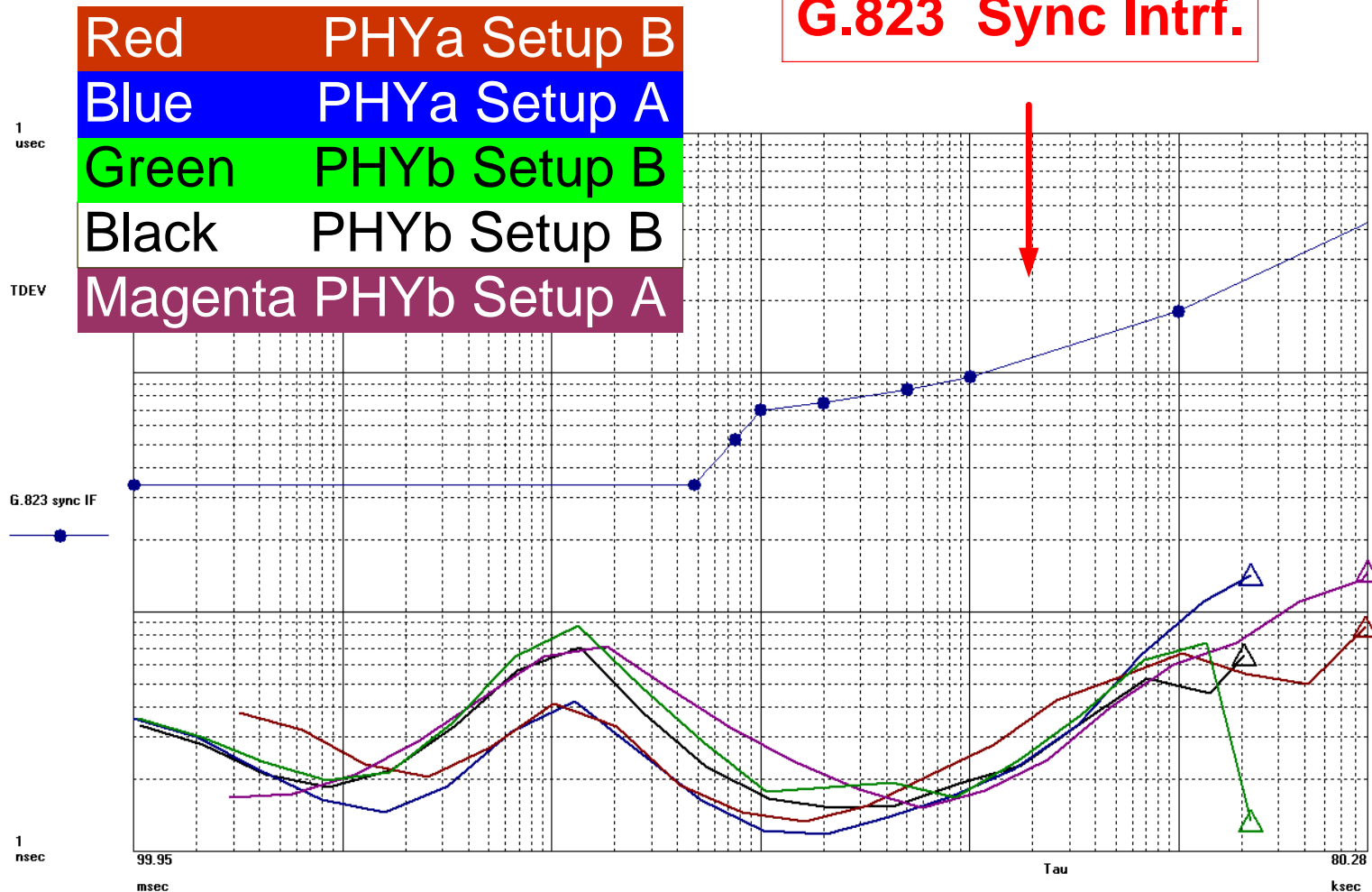
G.823 Sync Intrf.



PRELIMINARY RESULTS

TDEV: Sync Ethernet Results

G.823 Sync Infrf.



PRELIMINARY RESULTS

Conclusions

- Packet switched networks which provide common reference clock are happening now
- Differential timing is compliant with strictest performance requirements
- Differential timing is a robust and cost effective solution

Thank You

ITSF 2006